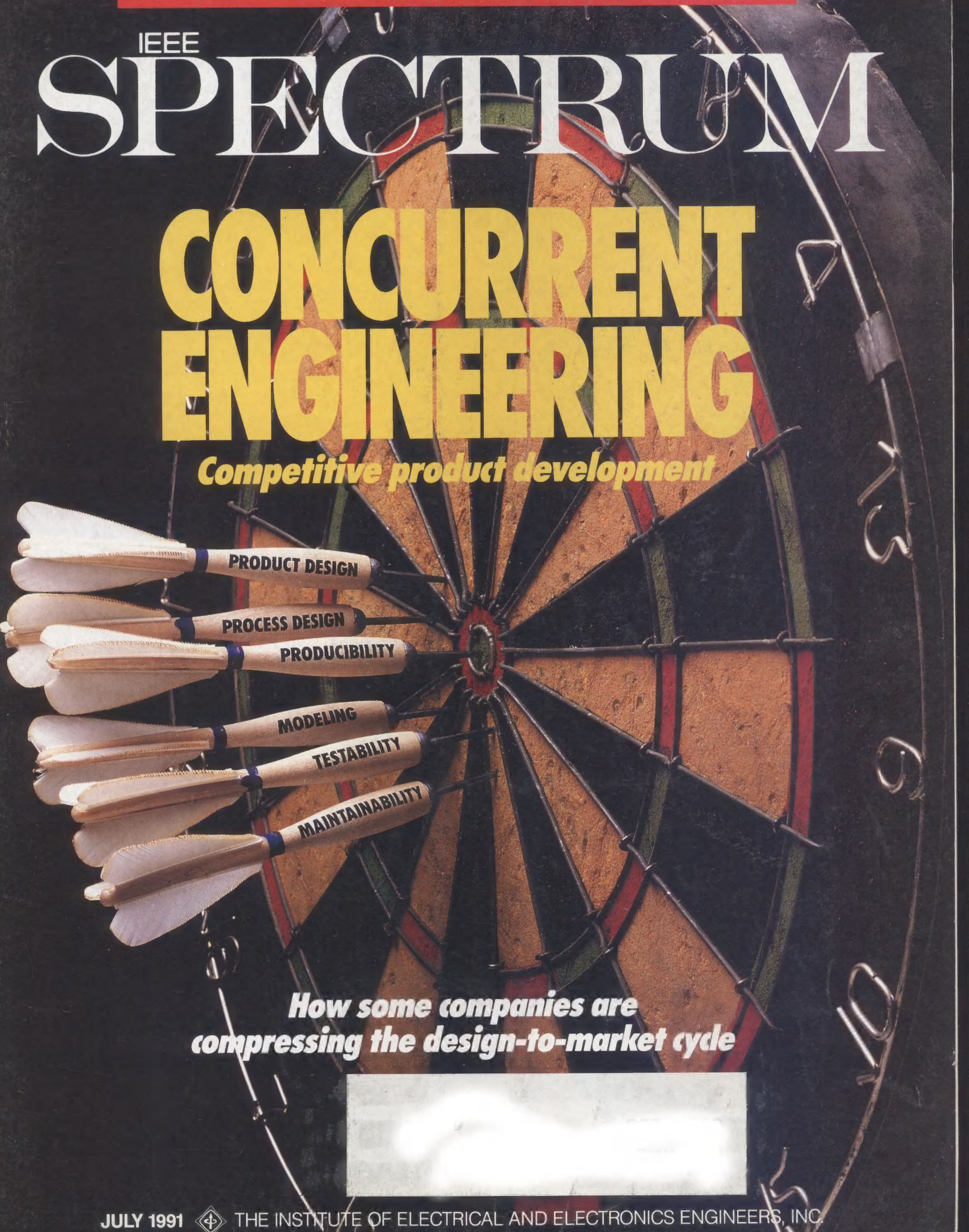
MATH COPROCESSORS P.38

IEEE
SPECTRUM

CONCURRENT ENGINEERING

Competitive product development



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SPEA 7/91

Newslog

MAY 8. Scientists at **BellCore,** Livingston, N.J., said they developed a technique for making high-temperature superconducting devices out of atom-thin layers of superconducting yttrium-barium-copper-oxide and non--superconducting praseodymium-copper and oxygen atoms. Immediate potential uses are in extremely sensitive radiation, microwave, and magnetic field detectors, the researchers said.

MAY 14. The **Economic Strategy Institute,** Washington, D.C., released a study showing that Japanese companies have made more than half of the foreign purchases of stakes in U.S. high-technology concerns during the last 2-1/2 years. The Japanese haul includes investments in 66 companies in computers, 41 in semiconductors, 27 in advanced materials, 25 in semiconductor equipment, 23 in telecommunications, and 11 in aerospace.

MAY 17. Astronomers at the Goddard Space Flight Center, Greenbelt, Md., said the **Hubble Space Telescope** had observed gas clouds circling a star, **Beta Pictoris** in the constellation Pictor, revealing for the first time the broad structure and dynamics of what could be a planetary system in the making. Scientists also reported that the Hubble's spectrograph detected the distribution of brief, intense flashes of gamma rays in regions relatively near the Milky Way—rather than farther out, as many astrophysicists had assumed.

MAY 20. General Electric Co., Fairfield, Conn., said it has won permission from the Japanese Government to proceed with a $1 billion contract to build the world's first two advanced boiling-water nuclear power reactors in Japan. **Hitachi Ltd.** and **Toshiba Corp.** will help to install the plants—an order worth $4.8 billion—at Tokyo Electric Power Co's Kashiwazaki-Kariwa power station.

MAY 23. The 17-nation **Coordinating Committee for Multilateral Export Controls** agreed to allow Western countries, led by the United States, to sell a vast array of high-technology items, including PCs, lasers for semiconductor manufacturing equipment, scientific instruments, and civilian aircraft, to the USSR and its former East European allies. But optical-fiber, night vision, and thermal imaging equipment remain closely controlled.

MAY 28. CHI Research Inc., Haddon Heights, N.J., released a study done for the Federal government that compared the technical strengths of 1100 companies worldwide through the number of influential patents issued from 1983 through 1989. Though U.S. companies led in patents (105 000) during that time, the analysis showed that the United States could be overtaken if Japan's advances continue at the same pace they did in that time frame (77 000 patents), a remarkable feat for a nation with a far smaller industrial base.

MAY 29. ICL PLC, the UK-based computer manufacturer in which Japan's **Fujitsu Ltd.** has a majority stake, said it would buy Finland's **Nokia Data,** the computer arm of Nokia Group, for US $400 million. The deal will give the combined company, employing 24 000 people worldwide with global sales of $4 billion, fifth place in Europe's $102 billion computer market.

JUNE 3. The **United States** and **Japan** agreed to a **new semiconductor pact** similar to the 1986 one due to expire on July 31. Under the new agreement, the target for the share of all foreign companies in the Japanese market was kept at 20 percent—a target still to be met. The pact, however, contained no timetable for reaching this level. The pact also calls for the United States to suspend import duties imposed on some Japanese products since 1987. The agreement will run for five years, with an option to terminate it after three.

JUNE 4. Thinking Machines Inc., Cambridge, Mass., said it reclaimed its title as maker of the world's fastest supercomputer by introducing a machine, the CM-200, that delivered 9.03 billion floating-point operations per second (gigaflops) in one test and 17 gigaflops in another. That beats the 8.6 gigaflops of the Santa Clara, Calif.–based **Intel Corp.'s** Touchstone Delta supercomputer, introduced a week earlier.

JUNE 5. Scientists at the **U.S. Department of Commerce's National Oceanic and Atmospheric Administration** said that a sun storm was disturbing the earth's magnetic field and threatening electric utility equipment and communication systems in the northern United States and Canada. The storm also exposed some satellites to such high levels of radiation that they may have malfunctioned briefly.

JUNE 5. The **U.S. Senate** passed by an overwhelming margin legislation to allow the **seven regional telephone companies** to manufacture equipment—an important step toward rewriting the antitrust ruling that broke up AT&T Co. in 1984. Although the measure now moves to the House of Representatives, the Bush administration said it would veto the legislation unless provisions are removed limiting foreign components and requiring production only in the United States.

JUNE 5. The space shuttle **Columbia** was launched in Cape Canaveral, Fla., for a nine-day mission of **Spacelab 1,** with seven astronauts, 30 rats, and 2500 jellyfish aboard. The crew will conduct what NASA called the most comprehensive biomedical studies ever done in space, including investigations of weightlessness, dizziness, and motion sickness.

JUNE 6. The **U.S. House of Representatives** voted to spend nearly US $2 billion next year on the **Space Station Freedom** after NASA agreed to freeze spending on all other space projects at their current levels. The 240-to-173 vote was made three weeks after a House Appropriations space subcommittee voted to end the project.

JUNE 7. Conductus Inc., Sunnyvale, Calif., said it had demonstrated the world's first IC made with high-temperature superconductors. The ultrasensitive magnetic detector chip has seven layers of materials, more than any other previous device made from the new superconductors.

JUNE 7. The Bush administration announced that the **United States** and **Japan** would ease their **export controls on supercomputers** to allies in Western Europe and the Pacific Rim. The pact requires export safeguards only for supercomputers doing more than 195 million theoretical operations per second. But the accord also tightens export restrictions for 30 countries that have yet to sign the Nuclear Non-Proliferation Treaty and for others that are suspected to be developing long-range missiles.

Preview:
JULY 11. The longest **total solar eclipse** until 2132 is expected to be visible around sunrise on the Big Island of Hawaii, around noon in Baja California and off the coast of Mazatlan, Mexico, and at sunset in Barra do São Manuel, Brazil. The event will have a totality duration of a 6-minute and 58-second maximum, just 33 seconds short of the greatest duration possible.

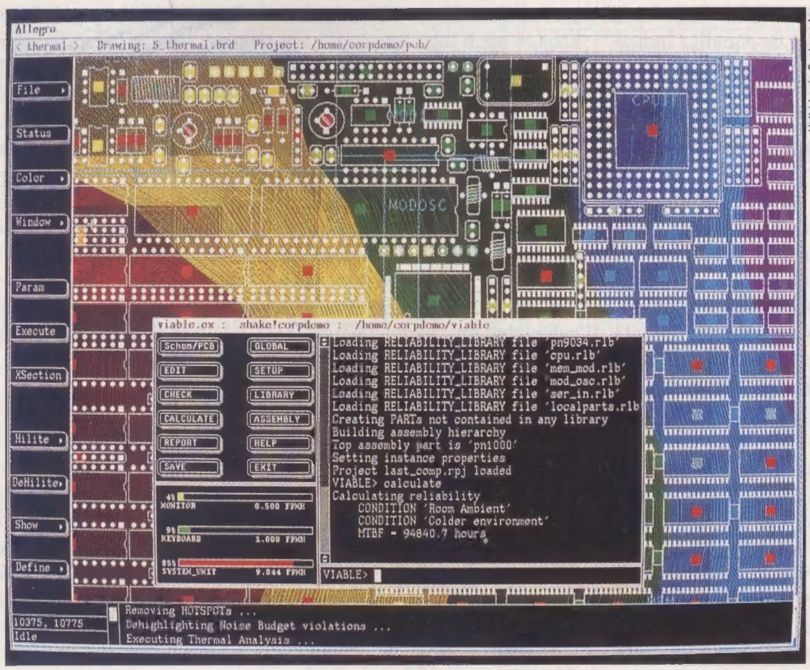
COORDINATOR: Sally Cahur

JULY 1991 Volume 28 Number 7

IEEE
SPECTRUM

SPECIAL REPORT: CONCURRENT ENGINEERING

Cisco Systems Inc.



Valid Logic Systems Inc.

A thermal, reliability, and noise analysis package displays the temperature distribution on a simulated circuit board. Such analyses are used to fix problems before a design is completed. The Defense Advanced Research Projects Agency (Darpa) seeks to integrate analyses of this kind with other systems in concurrent engineering.

ITEK Optical Systems Division, Litton Systems Inc.


Cyrix Corp.

Fractal images such as this view of a Mandelbrot set require intensive computations—and math coprocessors can help personal computers do them fast. The coprocessors also excel at simulation and data analysis, among other areas. The key: algorithms implemented in hardware.

Cover: Being on target with concurrent engineering means that all elements contributing to the success of a product must be simultaneously involved. Design by Gus Sauter, photographed by Chuck Kintzing. See p. 22.

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Reflections

Engineers: born or made

People often ask me how I became an engineer, as if to say, how did you pick up this terrible disease? Since no one asks lawyers and business tycoons how they became what they are, I feel some resentment. Imagine someone asking, "Mr. Trump, how did you decide to become a real estate magnate?" I could imagine the Donald reflecting for a moment. "Well, first I considered engineering," he replies. "But I decided that the potential for philosophical gratification and self-realization in that, ah. . . profession, was not, well, what I had come to expect."

Usually I'm bored with this topic, so when someone asks that question, I simply say that I was born an engineer. That cuts the conversation short, with the questioner nodding in apparent understanding. I can see the thoughts flickering across the faces of these people. "Of course," they are thinking. "What a terrible burden to carry through his life. Amazing that he turned out so well—considering."

In one of my responsibilities at work, I often had the task of introducing military generals as banquet speakers. I was always given an official biography, but they all seemed the same to me. (I suppose our engineering biographies look the same to generals, too.) Something that caught my attention, though, was that these biographies always began with "General Whatshisname was born in Abilene, Kansas."

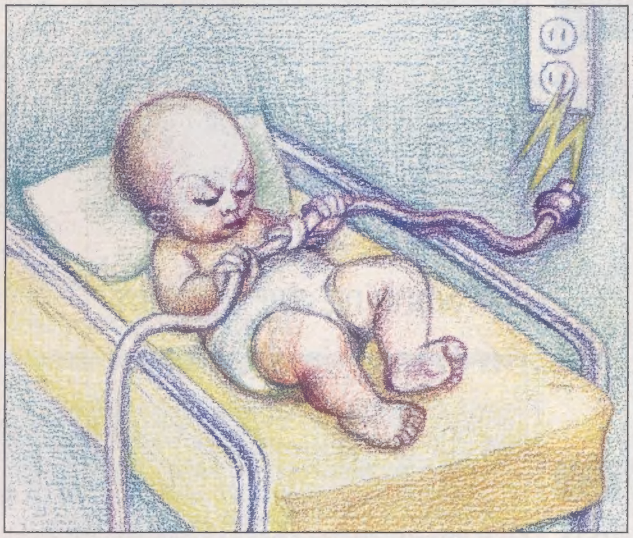
The concept of being born a general amused me. I would imagine the family and friends gathered around the baby's crib in Abilene. "Why just look at the little general!" they would exclaim. There would probably be three stars on the baby's diaper.

But instead, imagine the family that has just had a baby engineer bestowed upon them. As the expectant father paces nervously in the waiting room of the maternity ward, the swinging door opens and the doctor enters. He looks distracted, and avoids making eye contact with the anxious father. But as he hesitates in speaking, obviously trying to frame his words, the father leaps into the silence.

"Is it a boy?" he asks. There is a fractional pause—a kind of neutrality—in the doctor's silent expression. "Then it's a girl!" concludes the father breathlessly. By now the doctor has forgotten the comforting words that he had planned. There is the briefest negative shake of his head. "No, it's an engineer," he blurts out artlessly.

The father stiffens, resisting a display of disappointment. "You're . . . you're sure?" he stammers. "I'm afraid so," says the doctor in his most practiced, soothing voice. Now a frown creases the father's face as an afterthought suddenly occurs to him. "Is it a boy engineer or a girl engineer?" he asks timidly. For a moment the doctor seems uncertain. "I'm pretty sure it is a boy engineer," he says reflectively.

Several moments of awkward silence pass before the new father probes the doctor's uncertainty. "How can you tell—I mean, about the engineer part?" he asks. The apprehension on his face seems to invite a withdrawal of the diagnosis. But the doctor shakes his head firmly to cut short this futile hope. "You can always tell," he says. "The normal baby appears with a contented expression on its face—almost as if it wants to burst into song—whereas your typical engineer . . . well, I don't mean to imply that there is anything *abnormal* about an engineer . . . but they usually are frowning critically at the forceps. You can see their little minds ticking away, thinking about how they have to improve this place that they've come into."


Cathy Wassylenko

Amused by this fantasy, I polled some of my engineer friends to find out how they became engineers. "Do you feel that you were born an engineer, or made into one?" I asked. No one admitted to being born an engineer. Instead they would give almost identical stories. "Well, I always liked to play with radios (or some such mechanical or electronic gadget)," they would say.

Then they invariably finished with a note of pride. "I was always good in math and science," they said to explain why. It seemed to me their stories were tantamount to confessing to being born an engineer, but I suppose there are limits to self-revelation.

This matter bears on a problem our profession will face in the near future. Engineering will have to appeal more to women and minorities, and perhaps not everyone that the profession needs will feel that he or she was born an engineer.

One of my IEEE friends whispered a bit of heresy to me the other day. After glancing nervously around the room, he ventured an outrageous hypothesis. "Perhaps engineering is a trainable skill," he said. I composed my face into a shocked expression, and shook my head in proper admonishment.

Do you mean, I thought to myself, not daring to voice the words, that someone who hadn't been born an engineer—someone who hadn't played with mechanical and electronic things or hadn't necessarily aced the math and science courses—that such a person could actually be admitted to our sacred profession? What about our stiff entrance requirements and the series of tests and abstract mathematics courses that we have cleverly crafted for the early years of college? Only someone with innate engineering skills and total dedication to the profession could survive the weeding-out process. Only someone like us.

Sensing my disbelief, my IEEE friend hesitantly elaborated on his tenuous premise. "Suppose, just suppose, that we were to encourage people—maybe even nurture them—instead of just testing them?" he offered.

Well, this was going too far. Did this mean that a *normal* baby could actually become an engineer? My mind wandered back to the maternity ward, and now I imagined the doctor telling the new father that his wife has given birth to a healthy baby.

The father looks up in disappointment. "But we had hoped for an engineer," he says sadly. The doctor smiles, happy to be the bearer of good news. "You never know," he says. "Times have changed."

Robert W. Lucky

Calendar

Meetings, Conferences and Conventions

JULY

28th Nuclear and Space Radiation Effects Conference (IEEE Nuclear and Plasma Sciences Society); July 15–19; Town and Country Hotel, San Diego, Calif.; James R. Schwank, Sandia National Laboratories, Division 2144, Box 5800, Albuquerque, N.M. 87185; 505-846-8485.

LEOS Summer Topical Meetings on: Spaceborne Photonics: Aerospace Applications of Lasers and Electro-Optics (LEO/AES); July 22–24. **Optical Millimeter-Wave Interactions: Measurements, Generation, Transmission and Control** (LEO/MTT); July 24–26. **Epitaxial Materials and In Situ Processing for Optoelectronic Devices** (LEO); July 29–31. **Microfabrication for Photonics and Optoelectronics** (LEO); July 31–Aug. 2; Sheraton Newport Beach, California; Glenda McBride, IEEE/LEOS, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331; 908-562-3896.

Power Engineering Society Summer Meeting (PE); July 28–Aug. 1; Marriott Hotel, San Diego, Calif.; T.M. Winter, San Diego Gas & Electric Co., 101 Ash St., Box 1831, San Diego, Calif. 92112; 714-232-4252.

AUGUST

International Conference on Systems Engineering (AES); Aug. 1–3; Wright State University, Dayton, Ohio; B.A. Shenoi, EE Department, Wright State University, Dayton, Ohio 45435; 513-873-3527.

26th Intersociety Energy Conversion Engineering Conference–IECEC '91 (ED); Aug. 3–9; Boston Marriott Hotel, Boston; Patrick Bailey, Lockheed Missiles & Space Co., 1111 Lockheed Way (59-32-535), Sunnyvale, Calif. 94088; 408-756-4268.

Cornell Conference on Advanced Concepts in High-Speed Semiconductor Devices and Circuits (ED); Aug. 5–7; Cornell University, Ithaca, N.Y.; R.J. Trew, North Carolina State University, Electrical and Computer Engineering Department, Box 7911, Raleigh, N.C. 27695; 919-737-2336.

IEEE members attend more than 5000 IEEE professional meetings, conferences, and conventions held throughout the world each year. For more information on any meeting in this guide, write or call the listed meeting contact. Information is also available from: Conference Services Department, IEEE Service Center, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855; 908-562-3878; submit conferences for listing to: Rita Holland, *IEEE Spectrum*, 345 E. 47th St., New York, N.Y. 10017; 212-705-7569.

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...ooks

...pace, or space-art com-... a reminiscence on how ...e moon by former Na-...nd Space Administration ...n and a historical per-...d science fiction writer ...at more could one ask? ...e paintings will be famil-...ost of them are utterly ...those by the Soviet ar-...ok is a diplomatic first: ...on between artists from ...ers and leading space-...ingly illustrative of their the universe.

...ed differences—subtle, ...robably culturally signifi-... most part, the works of ...s are ebullient, some of ...o portrayed less idealis-...e exhausted cosmonaut Tired I Am," by Josef ... And in general, while ...ends to be almost pho-...nd geometrical, the Soviet art gives a greater sense of feeling for the canvas and the brush.

Moreover, the Soviet artists also tend to evoke more images of mythology—including racing wild white horses and angelic trumpeters—and even whimsy, such as the first snowman on Mars. They also seem to be slightly less shy about portraying women and children in addition to bizarre landscapes and proudly glistening machines.

In the Stream of Stars gives individual biographies of the more than 70 artists whose works appear—and so subtly that only after a while did it dawn on me that throughout the book the captions and biographies of the U.S. and Soviet artists are distinguished from one another by the color (navy or maroon) of bars above their names.

The text is as fascinating as the art. It is

Calen

Meetings, Conference

JULY

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AUGUST

International Conference

Books

East meets West

Trudy E. Bell

If you are at all interested in the world's space programs or science fiction, this is a beautiful book to receive as a gift (and one well worth the occasional unsubtle hint to ensure that you receive it). Paintings from renowned artists are stunningly reproduced in its glossy, large-formatted pages; even the paperback version makes no compromise.

In the Stream of Stars: The Soviet/American Space Art Book. *William K. Hartmann, Andrei Sokolov, Ron Miller, and Vitaly Myagkov, Workman Publishing Co., New York, 1991, 183 pp., $29.95 cloth, $19.95 paper.*

In addition to chapters by the four luminaries who edited the book (all well-known in the astronomy, space, or space-art communities), there is a reminiscence on how it felt to walk on the moon by former National Aeronautics and Space Administration astronaut Alan Bean and a historical perspective by poet and science fiction writer Ray Bradbury. What more could one ask?

While a few of the paintings will be familiar to aficionados, most of them are utterly fresh—particularly those by the Soviet artists. In fact, the book is a diplomatic first: the first collaboration between artists from the two superpowers and leading spacefaring nations, strikingly illustrative of their differing visions of the universe.

For there are indeed differences—subtle, but consistent and probably culturally significant. While for the most part, the works of both nations' artists are ebullient, some of the Soviets have also portrayed less idealistic moods, such as the exhausted cosmonaut in "Oh, God, How Tired I Am," by Josef Minsky [see photo]. And in general, while the U.S. artwork tends to be almost photographically sleek and geometrical, the Soviet art gives a greater sense of feeling for the canvas and the brush.

Moreover, the Soviet artists also tend to evoke more images of mythology—including racing wild white horses and angelic trumpeters—and even whimsy, such as the first snowman on Mars. They also seem to be slightly less shy about portraying women and children in addition to bizarre landscapes and proudly glistening machines.

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Books

highly personal—often written in the first person. Graphically, it also cleanly sets off the art and is printed in a large and readable, as well as aesthetic, font.

All in all, it is a book you are likely to pick up and thumb through many times—along with your family and friends.

Senior Editor Trudy E. Bell, who first got interested in space technology through astronomy and science fiction, co-edited Close Up: New Worlds *with Ben Bova (St. Martin's Press, 1977) and wrote a science-fiction novelette "Harem" with Ilil Arbel that was published in* Analog *magazine (March 1979).*

COORDINATOR: Glenn Zorpette

Recent Books

Embedded Controller FORTH For the 8051 Family. *Payne, William H.*, Academic Press, San Diego, Calif., 511 pp., $49.95.

Digital Design, 2nd edition. *Mano, Morris M.*, Prentice-Hall, Englewood Cliffs, N.J., 1991, 516 pp., $52.

Discrete Mathematics. *Biggs, Norman L.*, Oxford University Press, New York, 1989, 480 pp., $39.95.

Turbo C++ Disk Tutor. *Voss, Greg,* and *Chui, Paul,* Osborne McGraw-Hill, Berkeley, Calif., 1990, 503 pp., $39.95.

Investigations in Algebra. *Cuoco, Albert,* MIT Press, Cambridge, Mass., 1990, 623 pp., $29.95.

Using SCO UNIX. *The LeBlond Group,* Osborne McGraw-Hill, Berkeley, Calif., 1990, 610 pp., $27.95.

The Digital Connection. *Lebow, Irvin,* Computer Science Press, New York, 1991, 261 pp., $15.95.

VHDL. *Perry, Douglas L.*, McGraw-Hill, San Ramon, Calif., 1991, 458 pp., $39.95.

QuickC: The Complete Reference. *Feibel, Werner,* Osborne McGraw-Hill, Berkeley, Calif., 1990, 1092 pp., $29.95.

Adaptive Filter Theory, 2nd edition. *Haykin, Simon,* Prentice-Hall, Englewood Cliffs, N.J., 1991, 854 pp., $66.

Teach Yourself GW—Basic. *Albrecht, Bob,* Osborne McGraw-Hill, Berkeley, Calif., 1990, 408 pp., $19.95.

Running Windows, 2nd edition. *Stinson, Craig* and *Andrews, Nancy,* Microsoft Press, Redmond, Wash., 1990, 516 pp., $24.95.

PC MAGAZINE EDITORS' CHOICE
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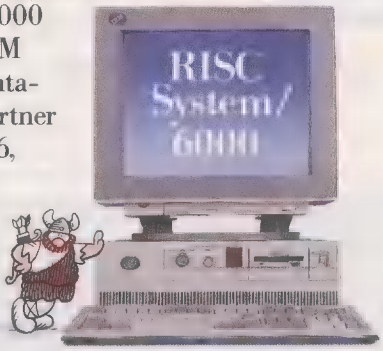


For the Power Seeker.

IBM

Calendar

(Continued from p. 8)

Sixth International Symposium on Intelligent Control (CS); Aug. 12–16; Key Bridge Marriott, Arlington, Va., Alexander H. Levis, Dept. of Electrical and Computer Engineering, George Mason University, Fairfax, Va. 22030; 703-764-6282.

International Symposium on Electromagnetic Compatibility–EMC '91 (EMC et al.); Aug. 13–15; Hyatt Cherry Hill, Cherry Hill, N.J.; Henry W. Ott, 45 Baker Rd., Livingston, N.J. 07039; 201-386-6660.

Neural Networks for Ocean Engineering Workshop (NN/OE); Aug. 15–17; Loews L'Enfant Plaza Hotel, Washington, D.C.; Patrick K. Simpson, General Dynamics–Electronics, 5011 Kearny Villa Rd., Building 70, Mail Zone 7202-K, San Diego, Calif. 92186-5310; 619-573-2417.

First International Conference on the Applications of Diamond Films and Related Materials (ED); Aug. 20–22; Auburn University Hotel and Conference Center, Alabama; Y. Tzeng, Department of Electrical Engineering, Auburn University, Auburn, Ala. 36849; 205-844-1869 or -2427.

Fourth International Vacuum Microelectronics Conference (ED); Aug. 22–24; Nagahama Royal Hotel, Shiga, Japan; Junzo Ishikawa, Department of Electronics, Kyoto University, Sakyo-ku, Kyoto 606, Japan; (81+75) 753 5325 or 5021.

Workshop on the Future of Electronic Power Processing and Conversion (IA); Aug. 28–29; Kruger National Park, South Africa; William Portnoy, Texas Tech University, Dept. of Electrical Engineering, Box 4439, Lubbock, Texas 79409-3102; 806-742-3533.

Region 10 Conference on Energy, Computer, Communication and Control Systems–Tencon '91 (C, COM, et al.); Aug. 28–30; Taj Palace Inter-Continental, New Delhi, India; K.R.S. Murthy, AT&T Bell Laboratories, Crawfords Corner Road, Room 2N-437, Holmdel, N.J. 07733; 908-949-4850; or H.L. Bajaj, B-101, Hillview Apartments, Vasant Vihar, New Delhi 110 057, India; (91+11) 360 412.

SEPTEMBER

Bipolar Circuits and Technology Meeting (ED); Sept. 9–10; Minneapolis Marriott Hotel, Minnesota; John Shier, 2800 E. Old Shakopee Rd., Bloomington, Minn. 55425; 612-853-3292.

Petroleum and Chemical Industry Technical Conference (IA); Sept. 9–11; Royal York, Toronto; Barry Wiseman, Reliance Electric Co., 5220 Creekbank Rd., Mississauga, Ont. L3W 1X1, Canada; 416-625-8112.

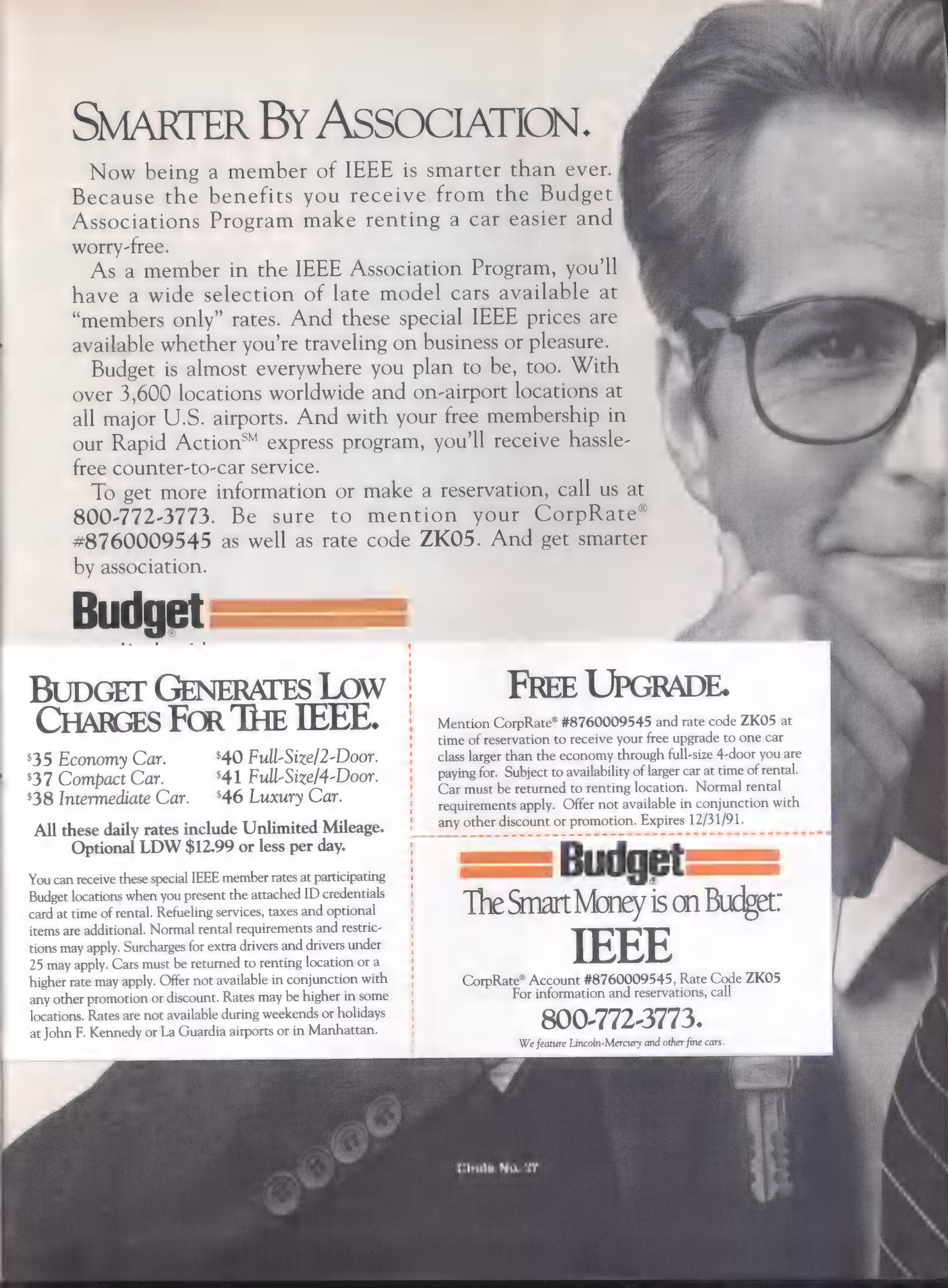
Third International Conference on Microstructures in Biological Research (ED); Sept. 9–12; Fort McGruder Inn and Conference Center, Williamsburg, Virginia; Martin Peckerar, Naval Research Laboratory, 4555 Overlook Avenue, Washington, D.C. 20375-5000; 202-767-3150.

11th International Electronic Manufacturing Technology Symposium (CHMT); Sept. 16–18; Le Meridien Hotel, San Francisco, Calif.; Bill Moody, 2529 Eaton Road, Wilmington, Del. 19810; 302-478-4143.

Seventh Multidimensional Signal Processing Workshop (SP); Sept. 23–25; Whiteface Inn, Lake Placid, N.Y.; John Woods, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, N.Y. 12181; 518-276-6079.

Autotestcon '91 (AES et al.); Sept. 23–

(Continued on p. 12J)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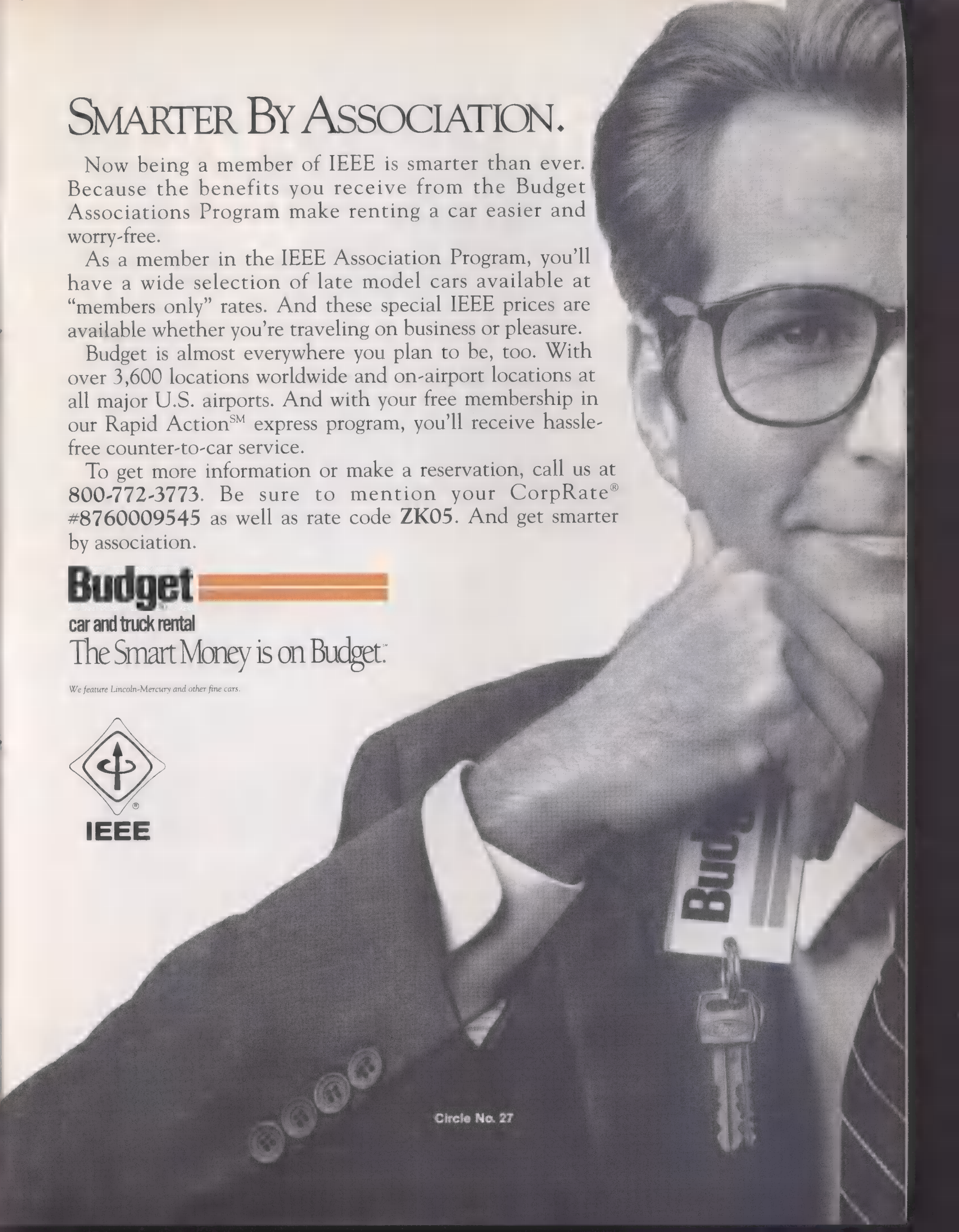
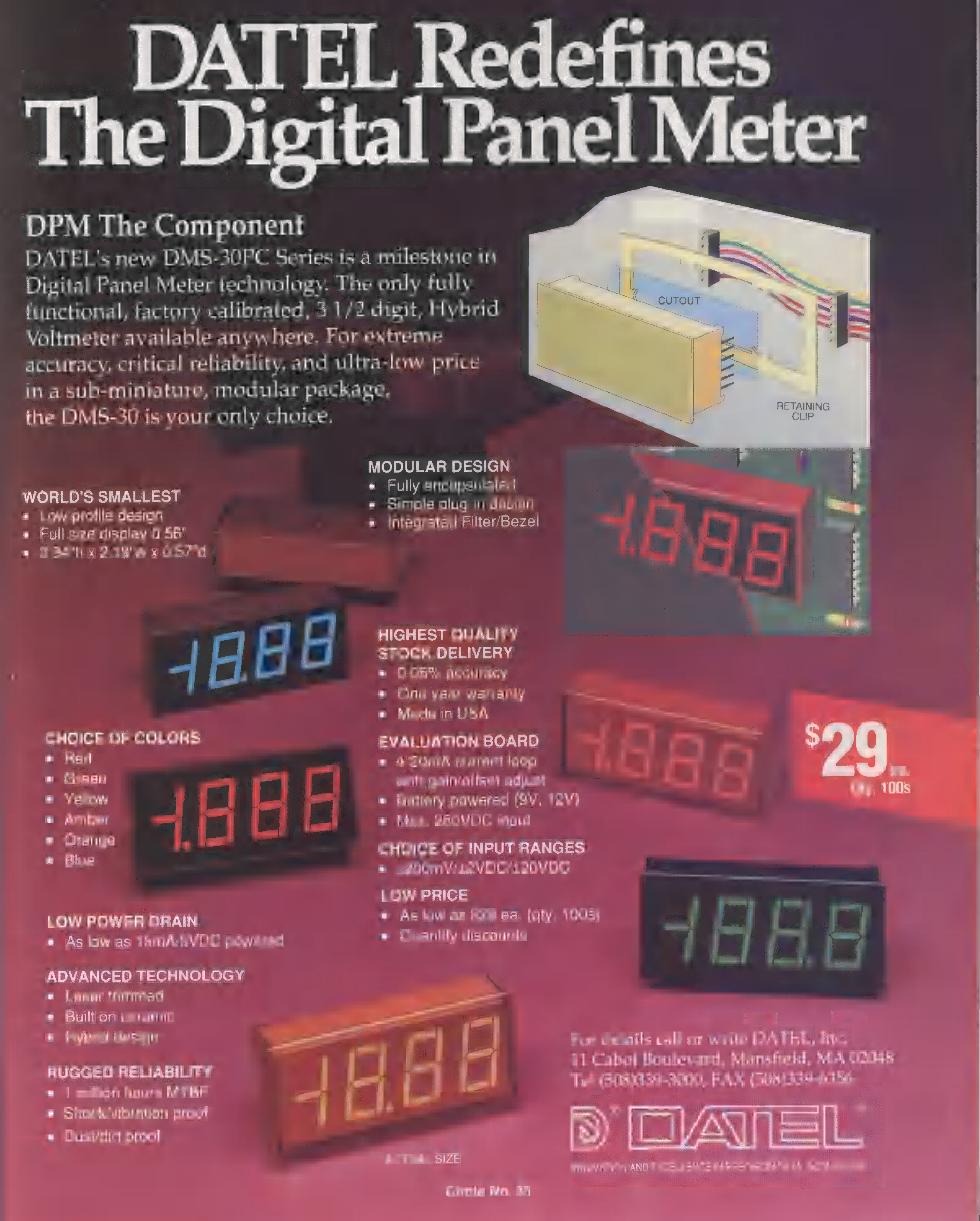
(Continued on p. 12J)



Circle No. 21



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Circle No. 33

Calendar

(Continued from p. 12D)

26; Disneyland Hotel, Anaheim, Calif.; Bob Rassa, Mantech International, 150 S. Los Robles Ave., Suite 350, Pasadena, Calif. 91101; 818-577-7100; fax, 908-222-5816.

18th International Conference on Computers in Cardiology (COMP et al.); Sept. 23–26; Venice, Italy; Corso Stati Uniti 4, 35020 Padova, Italy; (39+49) 829 5702.

International Symposium on Gallium Arsenide and Related Compounds (ED); Sept. 23–26; Sheraton Hotel and Towers, Seattle, Wash.; L. Ralph Dawson, Sandia National Laboratories, Division 1144, Albuquerque, N.M. 87185; 505-844-5678.

Fourth Annual International Application Specific Integrated Circuits Conference and Exhibit (IEEE Rochester et al.); Sept. 23–27; Rochester Riverside Convention Center, Rochester, N.Y.; Kenneth W. Hsu, Department of Computer Engineering, Rochester Institute of Technology, Rochester, N.Y. 14623; 716-475-2655.

Industry Applications Society Conference (IA); Sept. 28–Oct. 4; Hyatt Regency, Dearborn, Mich.; William Moylan, Moylan Engineering Associates, 13530 Michigan Ave., Dearborn, Mich. 48126; 313-582-9880.

OCTOBER

ICCD '91: VLSI in Computers and Processors (ED); Oct. 5–9; Royal Sonesta Hotel, Cambridge, Mass.; Dwight Hill, AT&T Bell Laboratory, 3D-446, 600 Mountain Ave., Murray Hill, N.J. 07974; 201-582-7766.

International Joint Power Generation Conference–IJPGC '91 (PE); Oct. 6–9; Town and Country Hotel, San Diego, Calif.; M. Scalice, American Society of Mechanical Engineers, 345 E. 47th St., New York, N.Y. 10017; 212-705-7053.

37th Holm Conference on Electrical Contacts (CHMT); Oct. 6–9; Marriott Downtown, Chicago; Conference Registrar, IEEE Inc., 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331; 908-562-3863.

22nd Photovoltaic Specialists Conference (ED); Oct. 7–11; Riviera Hotel, Las Vegas, Nev.; Howard E. Pollard, Ford Aerospace, 3939 Fabian Way, M.S. G45, Palo Alto, Calif. 94303-4695; 415-852-5131.

Fourth International Conference on Amorphous and Crystalline Silicon Carbide and Other III-IV Materials (ED); Oct. 10–11; Santa Clara University, California; Cary Yang, EECS, Santa Clara University, Santa Clara, Calif. 95053; 408-554-6814.

International Display Research Conference (ED); Oct. 15–17; Hyatt Islandia Hotel, San Diego, Calif.; Andras Lakatos, Xerox Corp., 800 Phillips Rd., Webster, N.Y. 14580; 716-422-9700.

GaAs Reliability Workshop (ED); Oct. 20; Doubletree Hotel, Monterey, Calif.; Anthony Immorlica, General Electric Co., Electronics Park, Building 3, Room 155, Syracuse, N.Y. 13221; 315-456-3514.

GaAs Integrated Circuits Symposium (ED); Oct. 20–23; Monterey Sheraton, Monterey, Calif.; S. Kuntz, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-347-5900.

(Continued on p. 44D)

GLOBAL VISION: FOR INTERNATIONAL CORPORATE INFORMATION NETWORKS.

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Global VISION opens the full range of advanced services. Facsimile and voice mail eliminate time zone problems. Distances disappear with international teleconferencing, remote CAD and high-speed file transfer.

High-quality NEC products form the heart of Global VISION systems. These include our advanced multi-media multiplexers, PBXs, packet switches and facsimile mail systems.

NEC invites consultation from corporations interested in Global VISION to reduce communications costs and improve productivity.

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The goal of worldwide telecommunications is free exchange of information throughout the global community. But North America, Europe and Japan all have different digital communication standards, and the digital networks of the nations involved cannot freely interconnect.

The network node interface (NNI) operating in the synchronous digital hierarchy (SDH) offers a clear solution. SDH is recommended by CCITT/CCIR and sets an international standard for high-speed digital transmission. SDH is the key to flexible broadband networks that feature efficient operation, administration and maintenance.

NEC is prepared to enter the SDH arena with new fiber optic transmission systems (FOTS) and digital radio products. The primary multiplexer combines tributary signals of 1.5, 2, or 6.3Mbps to 51.84 or 155.52Mbps. The high-order multiplexer bundles these composite signals up to 2.4Gbps. Cross-connector functions are also offered. SDH digital radios include 4/6GHz–150Mbps systems for long-haul use and an 18GHz–150Mbps system for short-haul use.

FOTS and digital radios with NNI are already in commercial service in Japan. FOTS based on SONET (the U.S. version of NNI) have been on field trial in the U.S. since 1990. SONET digital radios will go on trial this year in Australia and the U.S.

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Super Aladdin: Available only in Japan.

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NEC's answer to the growing need for fiber optics in the CATV industry is a 1.3μm distributed-feedback, laser-diode module. The OD-8339 improves picture clarity by reducing noise and distortions in analog CATV distribution.

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The OD-8339 comes with a single-mode fiber and a fine FC-PC or D4-PC connector. It provides stable operation over ambient temperatures from 0°C to 55°C.

Circle No. 9

Circle No. 25

Forum

Beaming watts from space to earth

The "Whatever happened to?" [March, p. 18] made me wonder what happened to the idea of converting solar generated power in space to RF and beaming it to earth, where it would be further converted to DC or frequencies useful in terrestrial applications. I remember thinking that the convenience and cost advantages of having solar power sources on earth was likely to make the terrestrial alternative economically more attractive than space siting for a long time. I also remember the environmental concerns about putting nuclear reactors in space.

The juxtaposition of these two approaches makes me wonder about two things. The first is whether terrestrially generated RF, beamed to space, rather than the other way around, might be a good way to provide power in some applications. The second is whether moderate average power requirements of space missions in general, compared to those of terrestrial power plants, might make the original space RF power source concept worth reconsidering for some applications.

Jerome Rothstein
Columbus, Ohio

Interested readers may want to review "Whatever happened to solar-power satellites?" [July 1983, p. 22]. —Ed.

No shortage of engineers

I have been receiving letters from "overqualified" engineers (read "overqualified" as over 40 years old) who have been unable to obtain gainful employment.

Many of the EE graduates may be or may have been IEEE members who were dismissed with little notice, sometimes after many years with a company. Among others, a manager of engineering at one company was replaced by two technicians, who were to attempt to do the same work. Others, after many years of service, have been discharged with two weeks' vacation.

There is no shortage of engineers, only of young, cheap engineers. We cannot afford to continue to treat engineers as a commodity to be hired and fired at leisure if we want to keep engineering work here.

The IEEE can help by recommending, among other things, the abolition of the industrial exemptions for use of PEs in high posts in engineering departments. An auto salesman today can be vice president of engineering, and will express the view I heard from an MBA at a recent symposium, "Don't let your engineers get close to your customers."

The MBAs and the bean counters are destroying engineering as a profession industrially. (Do not forget that an engineer can get an MBA degree with no trouble, but an MBA cannot qualify as an engineer without essentially a whole new degree program.)

I repeat, there is no engineering shortage. There is only a contrived shortage of low-paid junior engineers. Companies should be forced to give preference to older engineers, many of whom would take a job at a reduced salary in order to get gainful employment. If the IEEE cannot help engineers willing to work achieve professional status, the IEEE will have even worse financial problems than it does now. Can't the Institute see the handwriting on the wall?

Keats A. Pullen Jr.
Kingsville, Md.

Corrections

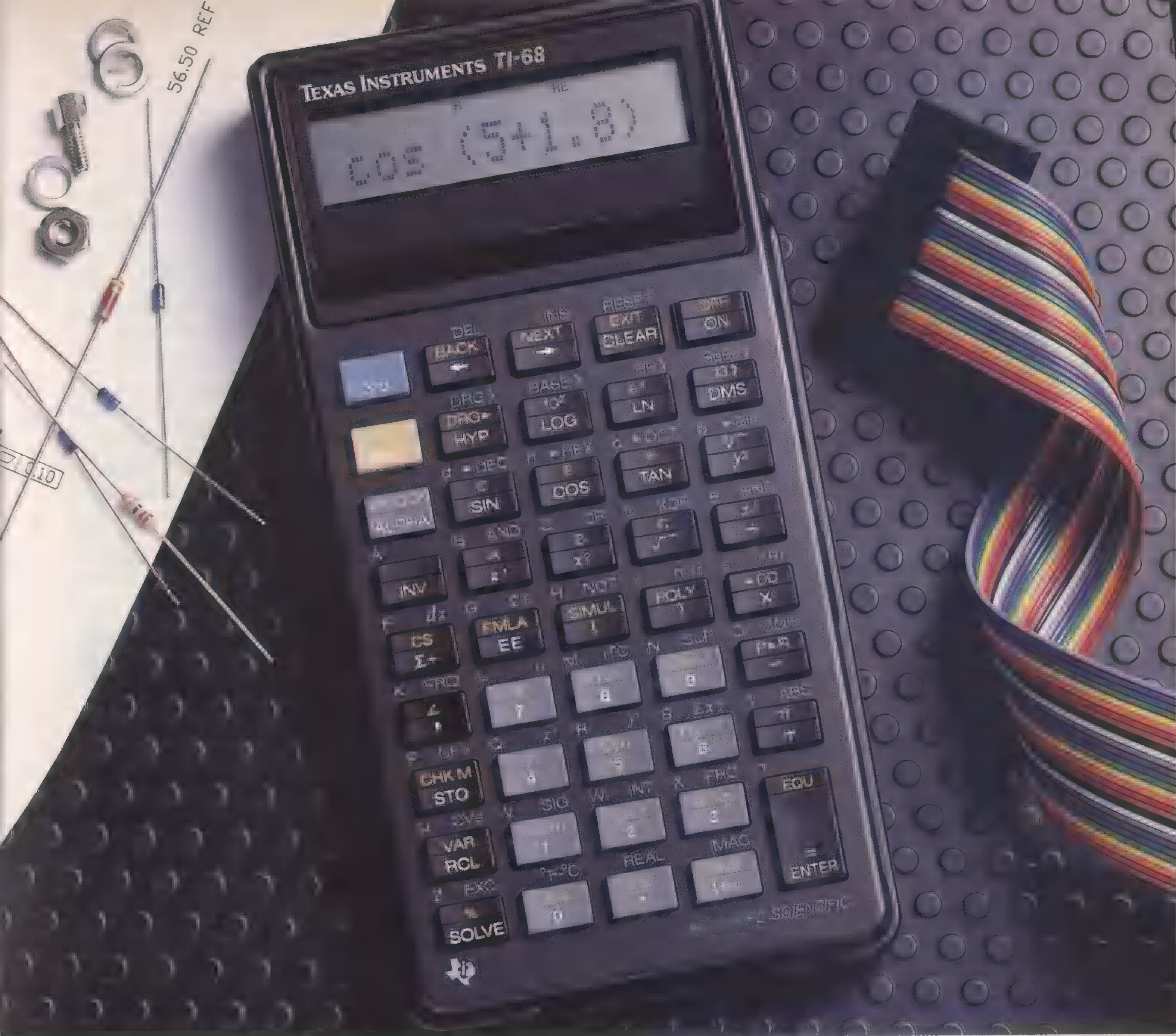
On p. 73 of the April issue, it was stated incorrectly that Masking-Pattern Adapted Universal Subband Integrated Coding and Multiplexing (Musicam) was the industry standard for broadcast digital audio. In truth it is one of two techniques being studied by the International Standards Organization (ISO). The other is Aspec, a multinational algorithm reflecting the work of AT&T Bell Laboratories, the Fraunhofer Institute in Germany, Deutsche Thomson Brandt of Germany, and CNET of France. The current stand of ISO, according to N. S. Jayant of AT&T Bell Laboratories, Murray Hill, N.J., is to merge features of Musicam and Aspec in a multilayer standard in which the more complex, higher layers permit lower audio-bit rates for a given level of audio quality.

On p. 38 of the May issue, in the middle of the second full paragraph from the bottom of the first column, the conversion from 0.75 inch should have been 19 millimeters.

In the last line on p. 29 of the February issue, "about 40 by 15 inches" should have been converted to "about 100 by 400 centimeters."

—Ed.

Readers are invited to comment in this department on material previously published in *IEEE Spectrum*; on the policies and operations of the IEEE; and on technical, economic, or social matters of interest to the electrical and electronics engineering profession. Short, concise letters are preferred. The Editor reserves the right to limit debate on controversial issues. Contact Forum, *IEEE Spectrum*, 345 East 47th Street, New York, N.Y. 10017 U.S.A.



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TEXAS INSTRUMENTS

Circle No. 24

Graphics

Finally: a benchmark for graphics

One of the most notable recent trends in computer science has been the adoption of benchmarks that are at once more standardized and more representative of the kinds of applications computers are actually used for. Now, several years after the proliferation of graphics-oriented workstations, that trend has apparently caught up with high-performance graphics.

Common measures of graphics performance include the number of vectors (line segments), shaded triangles, or polygons that can be drawn each second. But anyone who has ever tried to compare high-performance graphics systems from different manufacturers has probably been left with far more questions than conclusions. How long are the vectors? How big are the polygons? How shaded are they? How polygonal are they, for that matter?

Can I compare manufacturer A's polygons per second to manufacturer B's shaded triangles per second? Finally, does any of this actually have anything to do with my application? The answer to these latter questions is "probably not."

"The way to overcome this problem is to describe pictures," which is, after all, what graphics systems are designed to do, noted Carl Machover, president of Machover Associates Corp., a computer graphics consulting firm in White Plains, N.Y.

To develop a picture-level benchmark (PLB) with which to measure the performance of graphics systems, the Graphics Performance Characterization (GPC) committee was founded in 1986. The committee now includes representatives of such companies as Hewlett-Packard/Apollo, Digital Equipment, IBM, Evans & Sutherland, and Sun Microsystems.

Last April in Chicago, at the annual meeting of the National Computer Graphics Association, those five member companies released the preliminary results of benchmark trials run on their workstations (the Fairfax, Va.-based association has administered the committee since 1988). Results are reported in "GPCmarks," a normalized figure proportional to the reciprocal of the time required to run the benchmark—thus, a higher number means better performance.

The trials were conducted in five graphics categories: a two-dimensional printed-circuit board program typical of electrical computer-aided design applications [see photo]; a three-dimensional wireframe model of a computer chassis, which is rotated, panned, and zoomed; and three solid 3-D models, depicting an automobile engine's cylinder head, a human head, and the space shuttle. The last three display motion on various axes and illumination by more than one light source. Users evaluating workstations can make comparisons based on the category most like their own applications.

"There is no one good number for measuring graphics performance on a workstation," said David A. Cooper, technical director of the committee and a project manager at Hewlett-Packard Co. in Fort Collins, Colo. "Performance on different types of applications is so varied, and you can't just pick one number or average them together." Within a few months, he added, users will be able to convert their own applications into standardized formats, in effect making benchmarks out of them.

In the preliminary tests, the top speeds in the cylinder and human head simulations were logged by Hewlett-Packard Co.'s 730 TurboVRX (T4), while Evans & Sutherland Computer Corp.'s ESV 50/32 HC & LC Option workstation registered the best speeds in the other three categories. With six-figure price tags, the two machines were the most costly of the 25 tested. On the other end of the price scale, though, Sun Microsystems Inc.'s US $15 500 Sparcstation IPC GX matched or outdid more costly workstations on the computer chassis simulation.

IBM Corp.

The picture-level benchmark evaluates graphics workstations by timing how long they take to run five graphics programs. One program displays a PC board (above).

The PLB software, which was developed by Simgraphics Engineering Corp., South Pasadena, Calif., under the supervision of the Graphics Performance Characterization Committee, is available through the National Computer Graphics Association for $300. Annual subscriptions to the GPC committee's quarterly report, which contains tables of PLB results for the machines of various vendors, are available for $195 in North America and $225 elsewhere.

COORDINATOR: Glenn Zorpette

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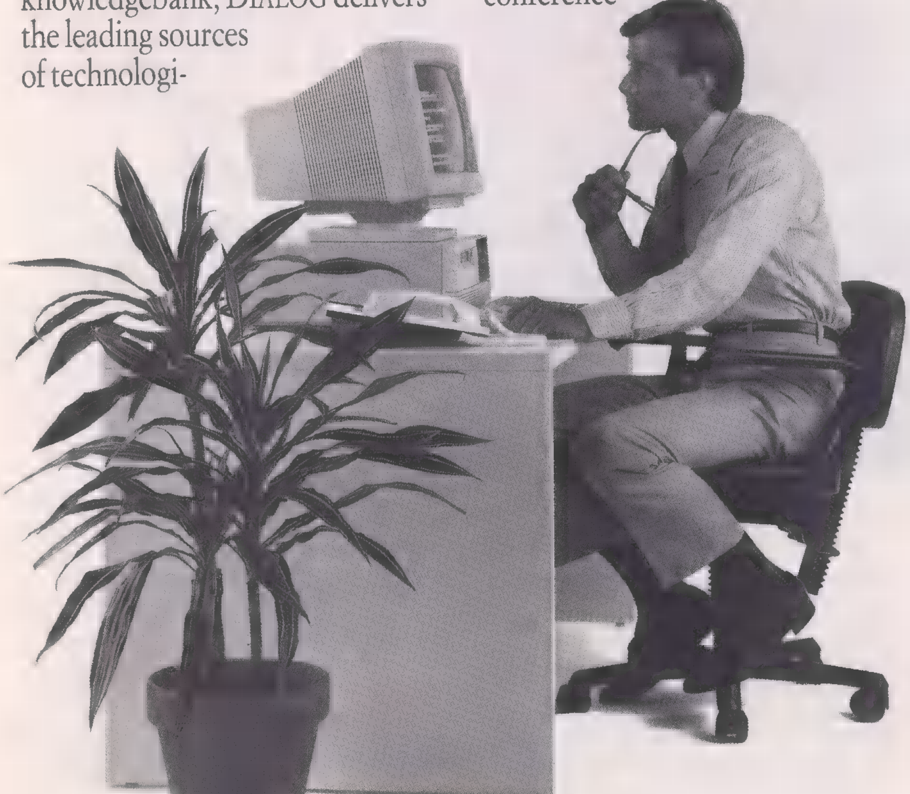

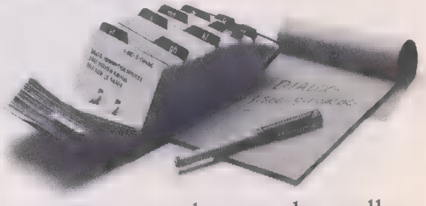

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JULY 1991 Volume 28 Number 7

Is college a commodity?

Inflationary costs are pushing most colleges and universities in the United States to an economic wall. The cost of room, board, and tuition at many private institutions exceeds US $20 000 annually. In some of those institutions, as many as 70 percent of the students require some form of economic aid.

Some colleges have adopted a needs-blind admissions policy, in which students are accepted on the basis of scholarship and other accomplishments without reference to financial need. The schools then help arrange a support package that may include scholarships, loans, and grants.

Even so, educational costs are rising so rapidly that the financial aids available cannot keep pace. Educators are projecting that in the foreseeable future nearly all students will require financial aid, and that a greater percentage of it will have to come from partially forgiven tuition (that is, direct grants from the universities themselves).

The complex task of allocating limited financial aid equitably to admitted students is an onerous one. It is carried out against the background of the annual ritual of mating applicants to schools, in which both sides "overbook." The admissions process can be costly, time-consuming, and wearying to the participants.

To help solve the problem, some 23 institutions in the Northeast have been sharing information on student financial aid and jointly reviewing the applications for such aid made by about 10 000 students who had been accepted to more than one of the 23 institutions.

Evidently this annual process has helped apportion scarce funds so that, at the bottom line, more qualified students could be supported by the participating colleges. What was required for it to work was a readjustment of mindset of the college administrators who traditionally were geared to compete strongly for the better students by using the enticements of grants and loans, irrespective of need.

Now the U.S. Department of Justice has stepped in with a charge that the process just described is a violation of antitrust laws. Attorney General Dick Thornburgh is quoted on the issue as stating that "Students and their families are entitled to the full benefits of price competition when they choose a college," and that "this collegiate cartel has denied them the right to compare prices and discounts among schools, just as they would in shopping for any other service or commodity."

First, to place a university education in the same category as a commodity on the face of it seems inappropriate. Choosing an education ought to be undertaken on a different plane from purchasing a Toyota or a Chevrolet.

Second, is it really unfair, in the context of the many similar social contracts endorsed by the U.S. government over decades, to provide more aid to those who need it at the expense of those who are well-heeled? Surely the fact that much of the funding in question is from private endowments as opposed to the public funds has no bearing. If anything, the private donors could withdraw their support if they deemed the appropriation process unfair. We know of none who did, even though the practice of cooperating on financial aid matters has been going on among some of the schools for decades.

Cathy Wassylenko

Bearing the brunt of the Justice Department's ire were the eight Ivy League members and the Massachusetts Institute of Technology.

The Ivy League colleges, Brown, Columbia, Cornell, Dartmouth, Harvard, the University of Pennsylvania, Princeton, and Yale, have signed a consent decree to avoid cooperating on financial aid in the future. MIT refused to sign the decree. Harvard's vice president and general counsel disagreed with the Justice Department's position, saying the practice "served the good social purposes of making sure that a limited amount of financial funds went to the neediest students." Princeton University's president said, "Awards in excess of need either divert resources from needy students or require an increase in revenues or reductions in other programs to support aid above the level of need." Columbia University, although it signed the consent decree, is reported to be considering asking Congress to pass legislation that would make cooperation specifically permissible.

Just when university coalitions in the United States are beginning to collaborate on important new ways to qualify precollege students for admission, retain college students through to graduation, and reform curricula, with the support in many cases of industry and the National Science Foundation, the Justice Department's reading of antitrust laws puts a chill on one important and time-honored cooperative program of some of those same universities.

In this important area, we must side with MIT's position that the cooperative procedures on financial support did not violate antitrust laws.

Should the issue enter the courts, we would then hope that Columbia University would be successful in its stated intention of pressing for legislation that would make the Justice Department's case moot.

Donald Christiansen

CONCURRENT ENGINEERING

The Boeing Commercial Airplane Group is using it to develop the giant 777 transport and expects to release design drawings a year and a half earlier than happened with the 767. John Deere & Co. used it to cut 30 percent off the cost of developing new construction equipment and 60 percent off development time. AT&T Co. adopted it and halved the time needed to make a 5ESS electronic switching system.

"It" is concurrent engineering (CE). These and other companies believe that their survival depends on it. In CE, the key ingredient is teamwork. People from many departments collaborate over the life of a product—from idea to obsolescence—to ensure that it reflects customers' needs and desires. Marketing, engineering, and manufacturing, for example, work together from the outset to anticipate problems and bottlenecks and to eliminate them early on. In so doing, they avoid delays in bringing the product to market and costly failures in service. Accounting and purchasing have their say, too, and help to ensure low product cost and reliable supplies of parts and materials.

With CE, no longer does marketing give product specifications as a *fait accompli* to engineering. No longer does engineering's design get "tossed over the wall" to manufacturing. Instead, all work together—in fact, one industry observer likened CE to "tossing the engineer over the wall."

CE is much more than teamwork, however. Computer-aided design, engineering, and manufacturing tools play a big role. Systems for sharing and managing design information are vital in large projects. CE also goes by other names like simultaneous or parallel engineering. Indeed, Japanese consumer electronics manufacturers have practiced it for years without giving it a special name; they consider it simply good business and engineering sense.

In this special report, experts present an overview of CE, give advice on implementing it, define key concepts, and describe efforts to foster its growth.

Alfred Rosenblatt Managing Editor
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New rules for world-class companies

Focus all resources so that new products work right the first time, rather than toss designs 'over the wall' for manufacturing to produce

Companies relying on traditional ways of designing new products and bringing them to market are being shocked into action by competition from world-class companies. Books, articles, and academic research have recently focused on the disparity that exists among companies in product development costs and cycle times, manufacturing costs, quality, reliability, and customer satisfaction. What their authors found was 99 percent common sense: they rediscovered the old adage: "Work smarter, not harder."

Many companies in Japan, the United States, and elsewhere are now doing just that. They compete successfully around the world because they have adopted a panoply of techniques for developing and manufacturing high-quality products that come under the heading of concurrent engineering (CE). This new wave of the new-product game starts with multifunctional teaming. But it also includes concepts and techniques whose acronyms spell out the new rules: design for manufacture (DFM), continuous process improvement (CPI), total quality management (TQM), and quality function deployment (QFD) [see "Defining terms," p. 24].

Integrating all these features, CE strives to create successful new products by bringing together as early as possible in the design cycle a company's resources and its experience in design, development, marketing, manufacturing, service, and sales. These capabilities are then focused on developing and manufacturing a high-quality, lowest-cost product that meets the customer's needs.

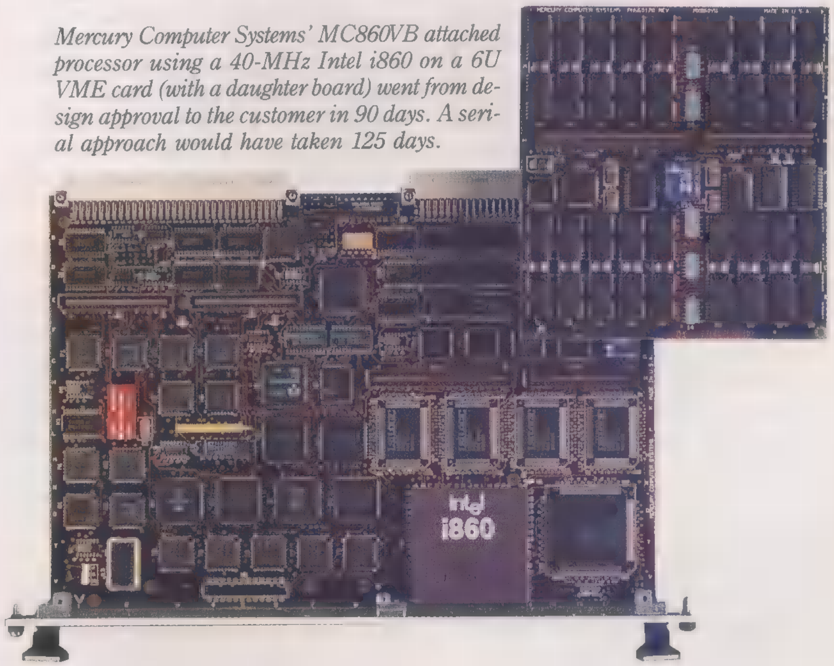
DOING IT IN PARALLEL. Most importantly, CE can shorten the overall product-development process because the steps along the way are handled in parallel instead of in series, as is usual. The time to market is also improved because CE reduces the number of product iterations. First prototypes not only meet spec, but also are compatible with the company's manufacturing capabilities.

An example from the Japanese automobile industry illustrates how CE can pay off. Measured by man-hours expended, the Japanese in the mid- to late-'80s took roughly just half the time U.S. companies did to develop and produce a new automobile. The results of this disparity were enormous. It meant the Japanese found it profitable to make fewer cars of any given model and keep it on the market for a shorter time. Overall, they could support a greater variety of products and target them toward more segments of the market. This strategy in itself could lead to still higher sales and profits.

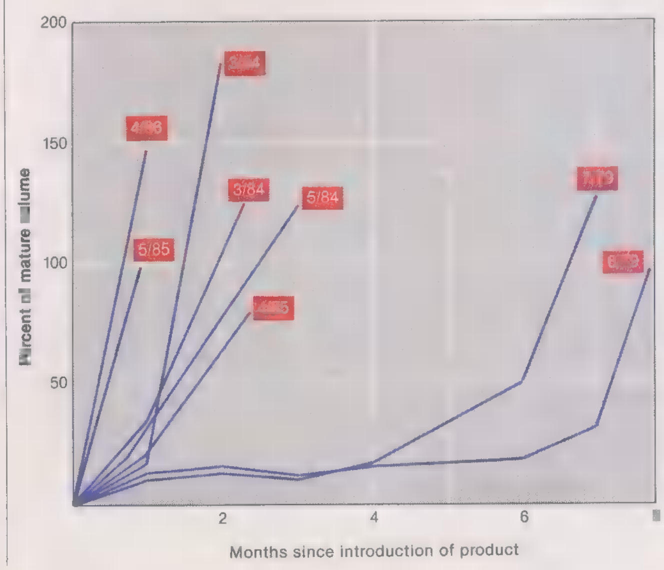
Since most of the profit from a successful product comes early in its life cycle, turning the autos over faster allows their retirement from the market at close to their optimum profitability. They could then be replaced by newer products that are even more responsive to customer demands and that are built with more advanced lower-cost technology. But getting everything right the first time is paramount because products having shorter lives do not allow companies time to correct design errors or to re-engineer products for lower cost or higher quality.

CE has also scored well at Mercury Computers Systems Inc., a Lowell, Mass.-based maker of add-on processor boards for VMEbus. The company was able to shorten appreciably the cycle for shipping a new board from design approval to a customer for testing down to just 90 days instead of 125 days it would otherwise have taken. This achievement is particularly notable because Mercury used a mix of in-house capability and outside suppliers to lay out, fabricate, and assemble the board, which incorporates a 40-MHz Intel i860 microprocessor [see photo]. The company bases its success on understanding its customers' needs, as well as its own and its suppliers' manufacturing processes.

OVER THE WALL. For most of their history, U.S. electronics companies have usually operated by tossing new products developed in their design groups "over the wall" to manufacturing. The product engineering and manufacturing departments then took on the task of ensuring that the product was manufacturable. Once that was established,



Mercury Computer Systems' MC860VB attached processor using a 40-MHz Intel i860 on a 6U VME card (with a daughter board) went from design approval to the customer in 90 days. A serial approach would have taken 125 days.



[1] As concurrent engineering is introduced and experience is gained with it, production ramp-up to high volumes will be faster, as indicated in these curves for a line of medical electronic instruments.

Sammy G. Shina University of Lowell

they manufactured it.

This process inevitably leads to rework. For reasons of manufacturability, for instance, part dimensions and tolerances might have to be changed. But there is another problem in this division of specialties: manufacturing will not know which dimensions and tolerances are critical to the performance of a product, nor which can be relaxed to improve the manufacturing efficiency and yield. Thus, only "make or break" manufacturing characteristics are changed—because it is better to accept a marginally manufacturable product than to jeopardize proven (during prototyping) performance to make the unit easier to manufacture.

Any changes also mean, in turn, that documentation, such as parts lists and configuration and assembly drawings, must be altered, too. Tooling may have to be reworked and contracts possibly renegotiated with suppliers.

Historically, once the product of most electronics companies got to the field, marketing and field service organizations recorded customer complaints about it and its performance versus advertised specifications. Some also considered service technicians' reports about repairs and defect rates of parts and assemblies. In many cases, however, companies have still not learned from their past mistakes. Often, they fail to set up communication links to notify the design and development departments of deficiencies discovered in the field.

This happens sometimes because many companies do not have the management skills, resources, or tracking systems to identify deficiencies. But engineers are also overwhelmingly biased in favor of fixing problems in current products, rather than in preventing future problems by finding and eliminating root causes in the underlying development process.

Thus, companies tend to turn out new products with the same (low) levels of customer satisfaction, quality, and cost. They end up fixing problems again and again, while patting themselves on the back for their knowledge and experience in solving the same *déjà vu* problems for each product. Problems of one generation sometimes turn up in the next.

Granted, attempts are being made to rectify these failings. But these include after-the-fact, post-production improvement programs. Or cost-reduction and value-engineering programs are introduced to redesign the product and reduce its cost or increase its quality after its release to manufacturing.

What may finally help are guidelines and examples of do's and don'ts in the design of parts issued by the manufacturing and field service departments. The problem with these lists, however, is that they are also thrown over the wall (in the opposite direction, of course). And they fail to reflect the dynamics of change within both design and manufacturing.

MOVE OVER, R&D. With concurrent engineering, new products are no longer the sole domain of the R&D department. Since from the very start of CE, product development must involve all parts of an organization, effective teamwork depends upon sharing ideas and goals beyond immediate assignments and departmental loyalties. Such behavior is not typically taught in the engineering schools of U.S. colleges and universities. For CE to succeed, teamwork and sharing must be valued just as highly as the traditional attributes of technical competence and creativity, and they must also be rewarded by making them an integral part of the engineer's performance evaluation.

In putting the techniques of CE into action, quality function deployment (QFD) methods are designed to listen to the voice of the customer. Once customer requirements are well-defined, product specifications can be focused on what the customer really needs. This is especially true for

Concurrent engineering: defining terms and techniques

Powerful methods for design optimization have become an important part of concurrent engineering practice. Whereas traditional design aids, such as design guides and checklists, focus on one area of concern, the new methods make it easy to hold a wide range of issues in view simultaneously during the design phase of product development. In essence, "bookkeeping" facilities arrange large quantities of information in a way that enhances the concurrent engineering team's ability to use it and to cross over functional boundaries.

In most cases, a central graphical element helps the team visualize the key elements and relationships in a multidisciplinary design solution. At present, the methods are executed with pencil and graph paper or software-based spreadsheets. In the future, they will be integrated with design automation tools, computer-aided manufacturing systems, and, above all, with information management tools meant specifically for concurrent engineering. With further computerization, it will become possible to store and reapply the results of the methods and the supporting data, hastening product improvement over several generations.

Whatever form they take in the future, these classic methods should be part of the concurrent engineer's lexicon.

QUALITY FUNCTION DEPLOYMENT (QFD). Known as the "house of quality" before it crossed the ocean from Mitsubishi Corp.'s Kobe shipyard and Toyota Motor Corp.'s automobile factories to North America and Europe, QFD is a pair of spreadsheets that relate subjective customers' desires (called customer attributes, or CAs) to quantitative engineering characteristics (ECs). Where CAs intersect ECs on the first spreadsheet, simple symbols indicate a positive or negative, weak or strong relationship. There is room for noting the importance of each CA and a quantitative measure of each EC.

> Ishikawa gave factory workers seven powerful tools to enhance their productivity and reduce product variability

The second spreadsheet forms the "roof" over the house of quality—it shows the relationships between ECs by linking the EC columns of the basic spreadsheet in a matrix much like a highway mileage chart. Again, simple symbols express the degree of relationship.

By touring a house of quality, an engineering team finds out which CAs are important (because either the customer wants them or the competition has them) and the set of ECs to be addressed to improve each CA. The team can also observe whether efforts to improve any one CA harm other CAs.

DESIGN FOR MANUFACTURE AND ASSEMBLY. DFMA is both a philosophy of design and a software package that alerts design engineers to the manufacturing implications of their work. Geoffrey Boothroyd, a manufacturing engineer, had the idea and with Peter Dewhurst, a software engineer, developed a family of application-specific computer programs. These DFMA programs are rooted in years of research. They supply quantitative data on such manufacturing parameters as machining rates, assembly times, and material properties. With them, a designer can estimate quickly and accurately the effort involved in manufacturing a design—before it is too late to consider alternatives. The software is available from Boothroyd Dewhurst Inc., Wakefield, R.I.

Unlike traditional component-by-component analysis of a system's producibility, DFMA never lets the engineer lose sight of the system for the components. It focuses on production cost so that part complexity can be traded off against number of parts and the difficulty of assembling them.

ROBUST DESIGN. Genichi Taguchi developed the concept of robust design at the Electrical Communications Laboratory of Nippon Telegraph and Telephone Co. between 1949 and 1961, and won Japan's prestigious Deming Prize for his efforts. Briefly, robust design minimizes less-than-optimal interactions among a product's parts caused by external factors such as manufacturing process variations, abusive operation (for example, running at reduced supply voltage), and the environment (for example, higher-than-rated humidity).

Robust design is not the same as rugged or con-

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evolutionary products, where the customer is aware of the choices and capabilities of what is already on the market.

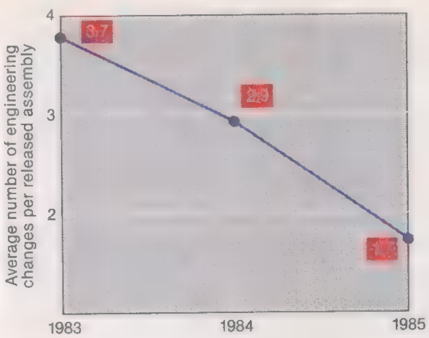
Certainly decisions like these, made during the concept definition and development phases of a new product, are highly leveraged and tend to have the greatest impact on overall life-cycle costs.

In manufacturing, with the help of total quality management (TQM) tools like statistical process control, CE can lead to product specifications and manufacturing tolerances that yield the lowest production costs and highest quality. Production rates can ramp up quickly to full volume after release to production because the manufacturing process is well-documented and controlled.

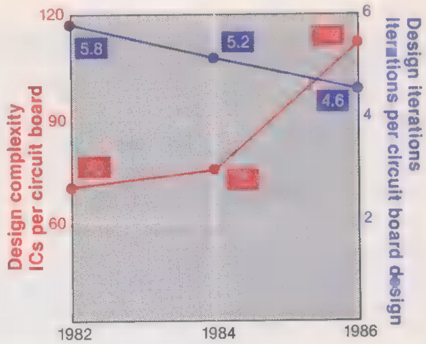
The important lesson to be learned is that CE methods, relying on the broadest base of company inputs, help to design the products right the first time. Moreover, by using continuous process improvement (CPI) techniques, CE does not lead to a plateau with respect to its benefits. Improvements will continuously be made when it comes, for example, to decreasing development time or ramping up production faster.

GAUGING RESULTS. The results of CE efforts can be gauged by comparing results gained with the new development process to those experienced with older products. Typical charts, shown here for an actual line of electronic medical instruments and normalized for a component count or percentage of first-pass yields, show increased efficiency in several areas:

- Shorter time for the product introduction cycle, as indicated by the production ramp-up to mature volumes [Fig. 1]. A quick ramp-up maximizes revenue from the new product, since the date of its obsolescence is likely to be fixed by competitive pressures and technology enhancements.
- Improved design quality, as measured by the number of engineering changes made within, say, six months after release [Fig. 2]. These engineering changes measure the design robustness and the completeness of documentation. (Data is normalized to the total number of released assemblies.)
- Reduced design iterations, taking into account the level of design complexity [Fig. 3]. For circuitry implemented on printed-circuit boards, the number of components is a good



[2] The application of concurrent engineering has led to fewer engineering changes after products are released to production.



[3] Another measure of concurrent engineering's payoff was that design iterations fell even as board designs got more complex.

servative design, which adds to the cost by using, say, heavier insulation or high-reliability components. Rather, robust design seeks to reduce product sensitivity to the sources of variability through careful selection of design values.

QUALITY LOSS FUNCTION. Variability reduction requires a very different mindset from that of traditional design and manufacturing engineering. The premise here is that any deviation from a product characteristic's optimum value, even though within tolerance, is costly. The quality loss function is an equation that Taguchi developed to calculate the cost; it says that the loss of quality increases with the square of the deviation from the target value. For example, the probability that two or more slightly deviant parts will combine to form a defective product—or one that fails prematurely—increases with the squares of the deviations.

The cost of quality loss shows up in various guises: warranty costs, costs of repair or replacement borne by the customer, and loss of customer satisfaction or good will.

SIGNAL-TO-NOISE RATIO. Besides minimizing deviations within a product, robust design seeks to insulate the product against outside sources of variability—"noise"—in manufacturing and use. The goal is to select design values that maximize the "signal" of key product characteristics in relation to reasonably expected "noise." Still, it is hard to select design values to maximize the signal-to-noise ratio. There are so many variations, and their interaction with design values is so complex, that the cost and difficulty of analyzing them seems overwhelming. For example, given 13 design variables, each subject to three kinds of variations (low, medium, and high), a total of 1 594 323 design options would have to be tried out.

EXPERIMENT BY ORTHOGONAL ARRAYS. To avoid massive experimentation, Taguchi introduced the orthogonal array concept. Several parameters are varied at a time in a pattern that changes from experiment to experiment (each pattern resembles an array of orthogonal vectors). This slashes the number of experiments by orders of magnitude—from 1.5 million for the 13-variable example to a mere 27. Orthogonal array experiments do not yield specific design values, but they do show how important each is to robustness, and a designer can then zero in on optimum values.

STATISTICAL PROCESS CONTROL (SPC). Quality by inspection depends on a certain level of defects so that their source can be pinpointed, and defects today are generally few and far between. So, rather than try to find defects in finished products, statistical process control seeks to monitor and correct drifts in quality in the manufacturing processes, starting with a thorough knowledge of the link between them and product defects.

ISHIKAWA'S SEVEN TOOLS. Kaoru Ishikawa embodied abstract mathematical SPC concepts in simple charts and graphs used by ordinary factory workers. He gave them seven powerful tools for enhancing their productivity while reducing variability in their part of the process: cause-and-effect diagrams, check sheets, histograms, Pareto diagrams, control charts, scatter diagrams, and binomial probability paper. Ishikawa took basic statistical tools and simplified and modified them to create a usable package. He conceived his ideas at the Kawasaki Steel Works in Japan in 1943 and later developed them as a professor at the University of Tokyo. For his work, he received Japan's Deming Prize and the American Society for Quality Control's Grant Award.

FISHBONE DIAGRAM. Ishikawa's cause-and-effect diagram—also called a fishbone diagram for its spine-and-rib structure—is particularly applicable to concurrent engineering. It starts with an effect (a dependent process or step) as a spine and works backward, with each major class of causes (influencing processes) added as a rib. Specific causes—or supplementary information on a cause—are added as branches on the ribs. The final diagram is imposing, but the design team can use it to study a seemingly incomprehensible array of causes and dependencies to find the critical ones.

The following terms also appear frequently in discussions of concurrent engineering:

CONTINUOUS PROCESS IMPROVEMENT. CPI is systematic continuous study of a process, year after year, to find ways of improving it. As applied to concurrent engineering, CPI reduces development time and final costs of products made by the process.

JUST-IN-TIME DELIVERY. JIT manufacturing methods provide components and assemblies as they are needed. They make it unnecessary to maintain large inventories, and thus help to cut costs.

TOTAL QUALITY MANAGEMENT. TQM applies a set of principles to focus continuous attention on quality at every step of design, development, and manufacturing by everyone in a company. TQM's overriding purpose is to increase value to customers.

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indicator of design complexity. Design iterations should go on declining even as the design complexity increases.

▪ Shorter production time, with the new product's assembly and fabrication operations reaching mature production faster. The learning curve of the improvement of production with experience should be less pronounced, or even nonexistent, for products developed using CE.

Another gauge of overall process quality is obtained by measuring and comparing yields. The yield for printed-circuit boards can be measured following board assembly and test, and burn-in. Typically the problems with board assembly arise from missing, misloaded, and reversed components, soldering defects, and defective incoming components.

CRANKING UP. In forming an interfunctional or interdisciplinary team, the best tactic is to set specific goals as early as possible. These should be aggressive, not evolutionary, and should be based on experience with current products.

For example, 10 percent improvement in new product cost, time to market, or reliability will not be adequate; the competition is likely to be shooting much higher. A case in point is Hewlett-Packard Co., Palo Alto, Calif., which in the 1980s instituted a program to improve the quality of its products in all respects by 1000 percent in five years. And it succeeded [see related article, p. 32].

The CE effort should combine computer-aided engineering and design and computer-integrated manufacturing (CAE/CAD/CIM) with design for manufacturing (DFM). It is vital here to:

▪ Document the capabilities and constraints of the current production process with structured analysis and data flow diagrams. Use them to eliminate redundant tasks.

• Review new parts and assemblies for manufacturability, serviceability, testability, and repairability. Be sure to include the traditional focus of design reviews such as technical correctness and overall quality.

• Develop an integrated computer network for downloading computer-aided design and engineering representations to the manufacturing equipment. This eliminates transcription errors in tooling up fabrication and assembly.

• Develop software tooling whenever possible so that manufacturing builds all prototypes. Manufacturing must assign the highest priority to producing them. Any discrepancies in assembly and fabrication instructions, violations of manufacturing equipment or process constraints, documentation errors, part misalignment, and part failures should be recorded. Manufacturability feedback should be supplied promptly to the design department together with the prototypes and suggested design changes. Such issues should be resolved further in formal manufacturability design reviews.

When producing prototypes, never use a special department, such as a model shop. These departments are staffed with very skilled people who can not only fabricate or assemble parts with incomplete information, but also make do with marginal manufacturing processes. Then when regular production sources are used, the parts may not be manufacturable to spec.

STRUCTURED ANALYSIS. As for structured analysis, many software packages are on the market for assisting in the drawing of structure and data flow diagrams. These charts' basic elegance is that they use only a few symbols and techniques to present a complex system or operation graphically.

Originally, structured analysis and design were tools for software developers who needed a means for making a hierarchical breakdown and description of software modules. The technique then replaced traditional flow charting as the magnitude of software projects and programming complexities went on increasing.

Now the charts use the hierarchical approach to illustrate a complex design and manufacturing task or information to be processed. They show the source and destination of the information flow that goes on. Often, the charts will highlight redundancies and inefficiencies in the system. Another advantage is that information flows between different systems and departments can also be presented graphically. Thus, the charts can describe the complex marketing, sales, manufacturing, and quality control systems used to develop and introduce new products to manufacturing and the marketplace.

Hewlett-Packard Co. decided to improve the quality of its products by 1000 percent in five years—and succeeded

ABOUT THE AUTHOR. Sammy G. Shina is associate professor of industrial technology in the College of Engineering at the University of Lowell, Mass. He has spent 22 years developing new products and state-of-the-art manufacturing systems. Most recently he was at Hewlett-Packard Co. where he held positions in manufacturing management, engineering, and R&D. He has written more than 30 technical papers in such areas as manufacturing automation, automated process development, and design guidelines for manufacture.

This article is based on material in Chapter 1 of Shina's recently published *Concurrent Engineering and DFM Electronic Products* (Van Nostrand and Reinhold, New York, 1991). ◆

The Darpa initiative: encouraging new industrial practices

A Government-industry consortium seeks to simulate small-team interactions among people in large, dispersed organizations

The purpose of the Darpa Initiative in Concurrent Engineering—DICE—is to encourage the practice of concurrent engineering in the U.S. military and industrial base. Toward that end, DICE's mission includes developing, integrating, and disseminating technologies for concurrent engineering. Studies and workshops in the late 1980s convinced Darpa it should borrow the best practices from industry around the world and apply them to weapons systems development, in particular the practice of considering all aspects of a product concurrently, including manufacturing and logistics, for the sake of high quality, low cost, and short time to market.

DICE was launched in 1988 by the Defense Advanced Research Projects Agency (Darpa) as a five-year program; US $60 million will have been expended on the program by the end of this year. A consortium of more than a dozen industries, software companies, and universities conducts DICE for Darpa.

The consortium's overall goal is to develop an architecture for concurrent engineering in which the people working on a project can instantly communicate with each other and access, share, and store up-to-date information in a transparent way, unhindered by geographic separation, organizational structure, product complexity, and incompatible tools, databases, and computing resources.

DICE is not concerned with developing techniques for automating the design and development process. These functions are well-served by computer-aided design and engineering software already on the market. Rather, DICE tries to give people working in large and scattered organizations the same

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freedom of interaction and information exchange as is enjoyed by a small team working in the same room.

PILOT PROJECTS. The concurrent engineering services are being developed in conjunction with several pilot projects. In one, General Electric Aircraft Engines, Cincinnati, Ohio, is implementing a concurrent engineering environment for a hollow airfoil for aircraft gas turbine engines. The goal is to be able to use novel materials and processes without the long lead time of sequential engineering and to accommodate production exigencies without losing the designers' intentions.

In another pilot project, Westinghouse Electronic Systems Group, Baltimore, Md., is re-engineering a signal-processing circuit board. The goal is to show the effectiveness of the DICE approach by examining the sequential development process, making it concurrent by sharing information among the engineering disciplines involved in the process, and measuring the improvement in reliability, cost, customer satisfaction, and development time.

Till now, GE Aircraft Engines has been the prime contractor for DICE, coordinating participants in pilot studies. Starting this year, Darpa assumes the prime contractor's responsibilities. West Virginia University's Concurrent Engineering Research Center (CERC), Morgantown, has led industrial laboratories and universities in developing generic services for concurrent engineering. The accompanying table lists other participants and their roles.

TIGER TEAMS. Product development is a cooperative enterprise in which groups of engineers, other experts, and managers work on different facets of the product under the direction of a project leader. In concurrent engineering, all these project members belong to "tiger teams"—interdisciplinary groups that rove across traditional department boundaries. Unconstrained by arbitrary barriers, tiger team members communicate their insights, make recommendations, and negotiate conflicts. They bring problems to light early.

DICE advocates using a set of computer-based services to enable a team, cooperating over a network, to transcend the barriers of distance, platform and tool heterogeneity, and insular viewpoints. Accordingly, the DICE services are designed for an information system that connects members of "virtual" teams by a high-speed computer network through which they communicate and coordinate information and workflows so as to promote cooperation and achieve rapid consensus.

In the past, computer-based information systems have tended to straitjacket people and isolate them. Different systems represent product data differently, lack program interfaces with each other, and provide no way of coordinating workflow. DICE aims to prevent this by emphasizing human factors as well as technology; technology can help greatly, of course, but an organizational commitment to team values is just as important.

Who's doing what in DICE*

Participants	Role
General Electric Aircraft Engines, Cincinnati, Ohio	Original prime contractor
Defense Advanced Research Projects Agency, Washington, D.C.	New prime contractor
Concurrent Engineering Research Center, West Virginia University, Morgantown	Leading industrial laboratories and universities in developing generic services
General Electric Corporate R&D Center, Schenectady, N.Y.	Developing techniques for integrating engineering tools and DICE services, modeling databases, optimizing designs, and managing constraints
Westinghouse Electronic Systems Group, Baltimore, Md.	Operating pilot site for circuit-board re-engineering
Cimflex Teknowledge Corp., Palo Alto, Calif.	Developing requirements manager and advisory tool for testability
Martin Marietta Corp., Baltimore, Md.	Supplying metal-matrix composites for airfoil pilot project
Howmet Corp., Whitehall, Mich.	Fabricating aircraft engine blades from metal-matrix composites
Bell Atlantic Knowledge Systems, Morgantown, W. Va.	Developing a high-level browser for object systems and neutral formats for data exchange
Carnegie Mellon University, Pittsburgh	Developing workstation and tools for representing and evaluating constraints
Rensselaer Polytechnic Institute, Troy, N.Y.	Developing shareable object data system and translating it into many computer languages
Stanford University, California	Developing techniques for managing risk and tradeoffs
North Carolina State University, Raleigh	Optimizing task schedules; developing programming languages to describe constraints
University of Maryland, College Park	Modeling product life cycles and electronics packaging methods
University of Iowa, Iowa City	Simulating performance of alternative design concepts for mechanical systems

*Darpa Initiative on Concurrent Engineering

The DICE services are based on existing standards such as X-Windows and TCP/IP data communication protocols and on commercial products such as spreadsheet and hypermedia software packages. These services are still evolving, and have many gaps (for instance, workflow control). Nevertheless, they are real. Documents exist on how to use DICE services. And they have been demonstrated successfully in an environment of multiple, geographically dispersed disciplines with many teams and covering the life cycle of a product.

CERC'S ROLE. West Virginia University's CERC operates one of the principal vehicles for accomplishing DICE's mission: a concurrent engineering testbed. The mechanical structures testbed, for example, is a small, integrated network of workstations and software packages (both commercial packages and those specially developed for DICE). It is used to design and develop complex mechanical prototypes, and even to machine them.

With the testbed, CERC can test and demonstrate DICE-developed technologies and evaluate new concurrent engineering technologies developed outside the program.

Among the general-purpose services it offers are transparent collocation of programs (any program in any workstation is available to other workstations as if it were hosted there); computer-based meetings, with text, voice, and graphics available by means of the network; a unified, shared product information base; and shared access to data in many object languages. Also included are "wrappers" (interface software for integrating engineering tools with the shared database and other services); browsing, via hypermedia, through data on the design intent and rationale; and "constraint" tools for managing customer requirements and enforcing design rules and process limitations.

In addition, the testbed offers many special-purpose services. For example, software-based "design advisors" provide guidance on casting, forging, assembly, testability, and so forth. Other special services include geometric modeling, finite-element analysis, and simulation of machining operations.

Another part of CERC's mission is to train people in concurrent engineering techniques. To do this, CERC has teamed with the Center for Entrepreneurial Studies and Development, also at West Virginia University, to teach people how to manage change and improve procedures. CERC also publishes monographs and handbooks, sponsors symposia and workshops, and participates in standards committees. It maintains CERCnet, a free electronic information ex-

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change system that provides subscribers with concurrent engineering abstracts and documents, concurrent-engineering-related bulletin boards, conferencing by electronic mail, and electronic want ads for those interested in related work.

TRANSFERRING METHODS. Finally, CERC participates in pilot projects that help both CERC and industry gain experience in transferring concurrent engineering methods into real-life situations, and help CERC evaluate DICE architecture services. The pilot project with GE Aircraft Engines seeks to shorten the time needed to develop a high-value mechanical component—a hollow fan blade in an aircraft gas turbine engine—and to make it more producible. The project with Westinghouse Electronic Systems Group focuses on a high-value electronic subsystem—a digital signal-processing board common to radar systems—and aims to make it less expensive and easier to tailor to a specific system.

CERC engineers and their industrial colleagues are carrying out both projects in this sequence of steps. First, they create teams and train them for the necessary change to a concurrent engineering culture. Next, the teams capture the "as-is" development process of the sequential engineering culture, and subsequently establish the concurrent engineering testbed, integrating in it DICE services, application tools, and databases. After that comes creating the "to-be" development process—the concurrent engineering culture—and setting up metrics for it. Then they implement improvements in the design and development process. Finally, they evaluate generic DICE services for integrated product development; validate that the requirements, features, and benefits of concurrent engineering are in fact realized; and document the case and the lessons learned.

So far, the needed improvements have been identified for both projects. Implementing and testing them are under way. The engineers have already written the to-be scenarios and chosen metrics. They have put workstations in place and connected them in networks and are installing DICE services in them.

Early experiences with both projects have been similar. For example, on both projects, a diverse group of DICE developers and pilot-site engineers and software specialists made up the team that both planned and accomplished the work. The DICE developers had to learn to follow their own precepts of team behavior and to share information early—other team members chided them for their diffidence in revealing their still-incomplete specifications for services. For their part, the other team members brought with them strongly held opinions.

What was expected to be a straightforward exercise in recording the current design-to-manufacturing process turned out to take nearly six months. Informal procedures had to be spelled out explicitly, with details of timing, data exchange, and sequence. The results fill a volume with diagrams.

The barriers of heterogeneity were faced immediately. For example, Westinghouse used older proprietary tools to which the communications services of DICE had to be added. A separate area was set up for a prototype testbed at Westinghouse, where team members from several disciplines could exercise the tools with DICE services. The pilot testbed was custom-tailored for the organization that would be using it. Eventually, it was integrated with Westinghouse's larger information management network.

Perhaps most important for the future, those CERC engineers who are also members of the faculty at West Virginia University are teaching new courses in concurrent engineering and are updating several standard courses to include this powerful concept. Moreover, plans are under way to offer a minor degree certificate in concurrent engineering as part of the master's degree program. It is high time, faculty members believe, that students experience close interdisciplinary teamwork with highly integrated information systems—the way they will be expected to work in the future.

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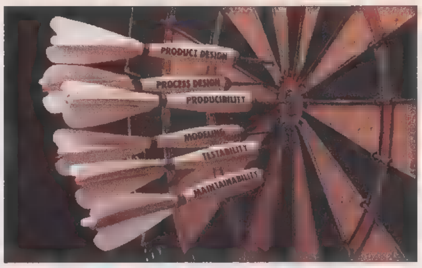
Ralph T. Wood is associate director of CERC. He was previously a program manager for GE Corporate Research and Development, where he led projects in product and process development. He has Sc.B., Sc.M., and Ph.D. degrees in mechanical engineering from Brown University, Providence, R.I.

K. Joseph Cleetus is a senior scientist at CERC. He previously worked on operations research applications of computers with IBM India. He has a Ph.D. in particle physics from the Massachusetts Institute of Technology, Cambridge.

A virtual 'tiger team' uses computers to leap traditional barriers and bring problems to light early



Making it work calls for input from everyone

Dedication, teamwork, and a sweeping corporate cultural change are essential for products ranging from one of a kind to high volume

Organizations implementing concurrent engineering (CE) stand to reap rich rewards. Better-designed, higher-quality products with a shorter time to market mean higher profits, and trouble-free product introductions often win market share away from competitors.

Starting and sustaining CE is not easy. It takes dedication and discipline, as well as a sweeping cultural change. Out goes the typical short-term business focus. In its place, a world-class CE culture zeroes in on continuous improvement. It relies heavily on teamwork among all employees connected with a product's development, plus close relations with customers and suppliers.

With CE, products can be rapidly customized by reusing engineering investments to meet changes in customer requirements, however frequent; order and factory cycle times are cut; up-front planning replaces back-end redesign, reaction, and rework; first-pass factory yields are above 95 percent; and people are interested in and proud of their jobs.

Implementing concurrent engineering is like putting a quality program into effect. It takes commitment by the entire organization, from top to bottom. It takes education at all levels so that everyone speaks a common language. It takes repetition: managers and engineers must constantly impress upon their peers, and those above and below them, their commitment to CE.

The serial organization of most companies hampers the communication needed for CE to work. The most obvious barrier is the separation of the various functions. Only once a design is verified, by either simulation or hardware prototyping or both, is it given to manufacturing, test, quality, and

Jon Turino Logical Solutions Technology Inc.

service engineers for review [Fig. 1]. Changes usually must be made. If done, they add to the development cost and time to market. If some are not done, because time-to-market pressure is great, or the design is behind schedule, the review merely acquaints the other specialists with the problems they will face later.

INTEGRATED EXPERTS. The CE organization, on the other hand, integrates the expertise from all the functions with the product design phase [Fig. 2]. Tradeoffs regarding ease of production, testing, and servicing are made along with product performance, size, weight, parts, and cost tradeoffs. Then, when a design is verified, the design is already manufacturable, testable, serviceable, and of high quality. The review is not likely to discover hard-to-solve problems.

In computer-aided engineering (CAE) the situation today is to have "islands" of design, manufacturing, and test automation. Some are linked well, some not so well. But progress is being made, even if front-end design tasks are easily the most popular with most vendors of CAE tools.

But CAE frameworks that support all engineering tasks are being considered. Also needed are synthesis tools that include expert-system rule checking for more mundane CE tasks (like designing for manufacturability, testability, and serviceability). It is heartening that professional organizations like the IEEE seek to standardize many of these items on frameworks that support open architectures. But until these tools are deployed, organizations practicing CE should press their design automation suppliers to develop items allowing for simultaneous simulation of both product and process designs. Systems must also allow for the networking of design databases to manufacturing process and control. (Some of this has already occurred in mechanical design.)

TOGETHERNESS DESIRED. Another nearly universal problem in getting CE under way is that the members of the product development team are not all in the same place and so are unable to communicate as fully as desirable. The best solution is to locate the members of the team near each other. This encourages ongoing communications—that is, not just at formal management and design reviews. It also fosters a group spirit of responsibility for seeing that the product gets to market as quickly as possible with the least amount of trouble.

It also helps to provide workspaces for everyone connected with the team, even for people in ancillary disciplines who spend only part of their time on the project. Those empty spaces will remind the others not to forget them and to seek out their input.

If the team members cannot all be in close proximity, they should at least have electronic communication with each other via an electronic network or commercial e-mail service. The ideal is a companywide network having a transparent user interface to a unified database. But any implementation that speeds two-way communications between team members is a step in the right direction. If ■ network is not feasible, the team should resort to "foot net" or "mail net"—transferring diskettes or modeming files to get input from each team member.

Alternatively, or sometimes in addition, the product development team may accompany the product as it moves through its design and development phases. This will teach all team members the consequences of their earlier decisions. This experience should prove applicable to the next product development. Team members will know which designs were easy to build, test, and service. They will also be in a much better position to reuse past designs, further cutting time to market and development costs.

OUTSIDE INFLUENCES. Another part of staying more competitive in the '90s is to get closer to both customers and suppliers. With customers, that means having not just the marketing and sales people closer but the product design team as well, so it will understand exactly what it should be designing.

Suppliers can also be valuable members of the product development team. It is almost always cheaper in the long run to buy something already available than to develop the designs, tooling, and manufacturing expertise oneself. Development efforts should be spent on the value that ■ company adds to the finished product and not on the ordinary components that go into it. The exception to this, of course, is where proprietary component technology or processes are involved.

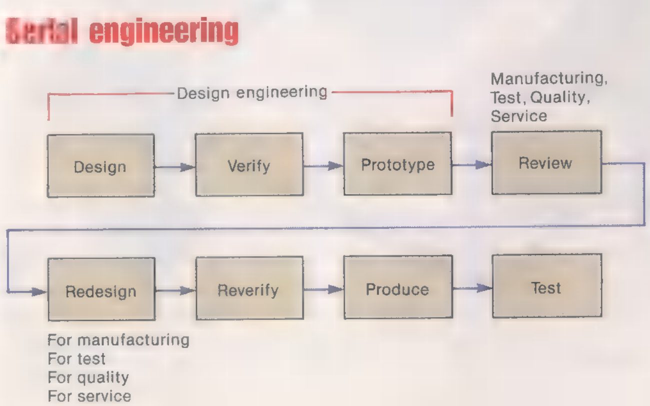
Working closely with suppliers adds their expertise at little or no cost. They can often suggest better, less expensive ways to do things. Tying them into an organization's technology and production needs also speeds design and facilitates just-in-time manufacturing practices. Reducing the overall number of suppliers also lowers the overhead costs of purchasing, inspection, and record-keeping. Supplier information also can be useful for estimating costs early in a project's design phase.

Note, too, that costs and other data constantly being developed by manufacturing, test, quality, and service functions should be applied to a new product's development. As these facts, which can affect the design itself, are developed, they should be used wisely for the improvement, not punishment, of other organizations (or, worse yet, of people). That means saying "If we do this the same way again, the following will result. If we do it with the CE discipline, we have the chance to..."

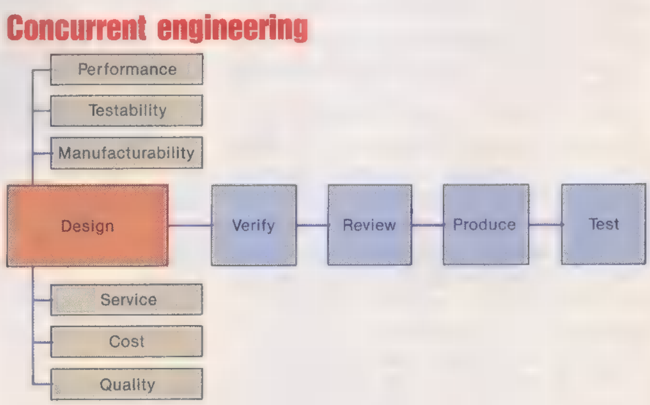
Never say, "Your last design was a disaster. Look at these numbers..."

If customer requirements dictate ■ design approach outside ■ company's capabilities, everyone needs to know, so that plans can be made to cope with it. An outside source may be required, or the approach will have to be modified to fit company capabilities.

In short, forethought and planning must extend much farther than has been customary. Shorter product life cycles and pressure for shorter time to market now make it imperative to renounce a philosophy of "redo until right" in favor of a philosophy of "right the first time." What does "right" mean? It comes down to the proper set of design tradeoffs for the success of the product (and also the business), in the light of



[1] Serial engineering is characterized by departments supplying inputs to design only after a product has been designed, verified, and prototyped.



[2] During product design, CE draws on various disciplines to trade off parameters such as manufacturability, testability and serviceability, along with the customary performance, size, weight, and cost.

what the customer wants, what the company can handle and what competitors can offer.

ABOUT THE AUTHOR. Jon Turino (M) is president and chief executive officer of Logical Solutions Technology Inc., a consulting and seminar firm he founded in 1978. He is the author of four books and hundreds of papers on the topics of concurrent engineering and design for testability. Prior to Logical Solutions, he held design and test engineering, customer support, and senior management positions at Xerox, Fluke Manufacturing, and Instrumentation Engineering. ◆

Success stories in instrumentation, communications

Case history 1: Hewlett-Packard

Small-work projects: teamwork counts more than computer-based tools

Anyone reading the current literature about concurrent engineering (CE) can easily get the impression that, to use the technology, a company has to make a big investment in computers and software. Certainly, computer tools help. But they are not indispensable, especially on a small project where the product is not a complex system but an item of electronic equipment such as an oscilloscope or logic analyzer.

What tools does an engineer need to get started in CE? Pencil, paper, some intelligence, and a willingness to work with peers in other functional areas to get the job done. Computer-based tools can be added as the budget permits.

That is how Hewlett-Packard Co.'s Colorado Springs Division started in 1980. Our development process was not even called concurrent engineering then, although that is what it was—and is. The process evolved naturally out of the need for increased cooperation between the various functional areas of the business as HP focused on improving manufacturability and reliability. The company had already adopted the continuous process improvement (CPI) philosophy—a devotion to constantly looking for a better way to do things This formed a solid base for CE efforts.

Roy Wheeler
Hewlett-Packard Co.,
Colorado Springs Division

Practicing CE has yielded remarkable results. A case in point is Hewlett-Packard's 54600 oscilloscope below. We knew from the start that cost would be a critical issue for this product. Intended as a general-purpose "personal" scope, this 100-MHz–bandwidth instrument would be competing with inexpensive Asian-manufactured units. Therefore, we wanted it not just to be price-competitive, but to offer greater functionality, too.

IN ONE-THIRD THE TIME. From idea to finished product, it took us about one-third the time to complete this project that it would have without CE.

Moreover, with CE, we were able to deal successfully with several complicating factors. First, there was our concern about keeping costs down. Here, materials engineering and manufacturing engineering made big contributions—materials engineering by advising designers of their choices of components, and manufacturing engineering by becoming closely involved in the design process and by providing an on-board integrated test system so that the unit could be priced at rock bottom.

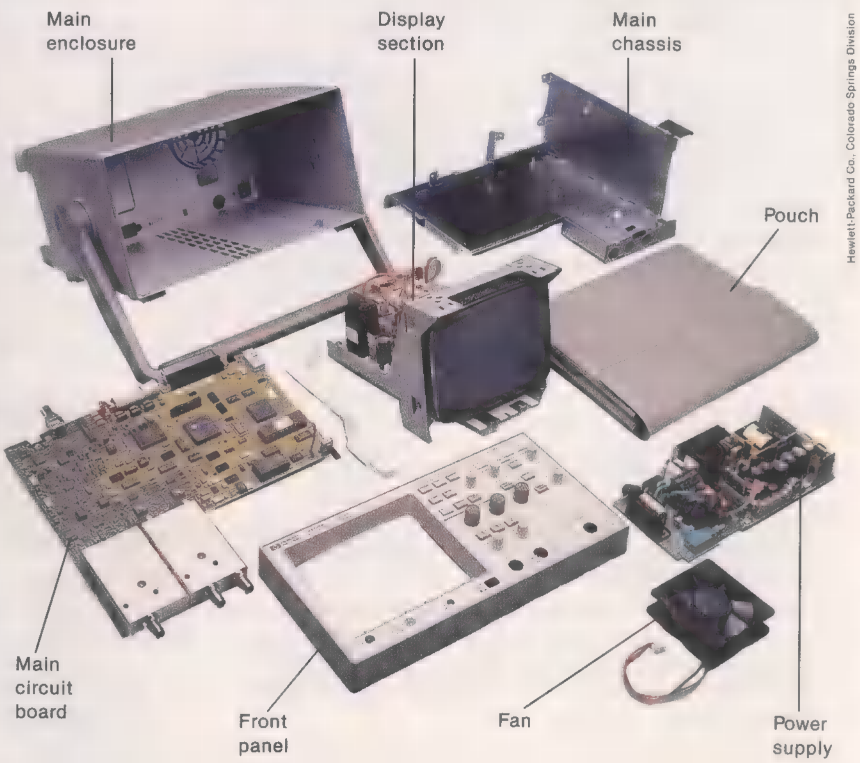
Other complications included surface-mounting all components, designing the unit with digital rather than analog circuitry, and meeting military specifications for low electromagnetic emissions. Often, these requirements were at odds with one another.

For example, a circuit engineer had just revised a critical digital circuit to boost its performance. The team's electromagnetic compatibility engineer tested the circuit and found that it radiated strongly. The two engineers working together found a solution. Without concurrent engineering, however, the problem would not have been recognized until much later, when it was time to test the circuit. By then, the circuit would have been committed to hardware, and circuit board masks would have been designed and fabricated. Undoing these preparations for manufacturing would have resulted in a waste of time and money.

The net result of our CE is that we produced the oscilloscope at the price we aimed for. Our cooperative effort made it possible to package the components in just a few modules that can be assembled into a complete unit in less than 18 minutes.

As in our development of the 54600 oscilloscope, the first step in any of our CE projects is to organize people from all sections of the division into project management teams under the leadership of the R&D project manager. Some team members are assigned to a project on a full-time basis, and others are assigned to several teams at once.

Usually, marketing and R&D start out the process by defining what the product should be. Manufacturing and reliability engineers join in when early implementation decisions are being made. To select sources and tech-



The concurrently engineered 54600 digitizing oscilloscope comprises only a few modules, all designed for fast assembly to keep manufacturing costs low. The pouch rests on the main enclosure and holds probes, cables, and the user's manual for the instrument.

nologies, purchasing and materials engineers come on board, while accounting provides cost and investment information as appropriate.

At one point in our evolving concurrent engineering, we called ourselves spider web teams since our goal was to catch all defects in production and the field and eliminate them. We had by then established total quality management (TQM), and drew service engineers into our teams because of their closeness to customers.

KEEPING PART-TIMERS CURRENT. One of the difficult things about applying CE to small projects is ensuring that part-time team members are productive on other projects when the team does not require their services, but that they are immediately available when their services are needed.

For example, a typical small project might need two to five design engineers full-time, half of a production engineer, one-third of a quality engineer, 10 percent of a buyer, 20–40 percent of a materials engineer, 10 percent of a cost accountant, 10 percent of an electromagnetic compatibility (EMC) engineer, and so on. A problem can occur if the project manager fails to recognize the need for the part-timers' help at the appropriate time, or if the part-timers are not fully aware of the latest issues when they are called on for help. There is a danger, too, that part-timers may become engrossed in certain projects, to the neglect of their other projects.

Early on, the group at Colorado Springs found a way to handle this problem. The trick is to include part-time members in all team-building activities at the outset, to invite them to all project management team meetings as the project progresses, and to make sure they receive copies of all project memos—electronic or paper. At Colorado Springs, part-timers are expected to maintain a level of currency with all their projects so that they can answer questions and make suggestions almost instantly.

Of course, safety engineers and EMC engineers are spread more thinly than others. Since they may work on as many as 12 projects at once, they can hardly be expected to attend a dozen team meetings a week. This means the project manager has to work especially closely with these people to keep them up-to-date and to alert them to meetings of particular importance to them. Agendas should be distributed several days before meetings so the multiproject engineers can decide which of them to attend.

HOW NOT TO ENGINEER. All this contrasts sharply with the author's experience in sequential engineering days, before joining Hewlett-Packard. As a design engineer for a large, well-managed manufacturer of electrical and electronic products, I learned of a new product only when marketing gave me a complete product specification. My colleagues and I proceeded on our own to design the product according to our interpretation of the specification. Then we negotiated changes with marketing, usually in an adversary relationship rather than in a spirit of cooperation.

Our design was then turned over to preproduction engineers, who modified the product to accommodate their manufacturing processes—also after much wrangling and haggling from us designers. Preproduction engineering handed off its work—including production tooling—to the production manager, and further conflict ensued as the design was adapted to the realities of production. Clearly, this is a time-consuming and wasteful way to develop a product.

Incidentally, the Colorado Springs Division uses many computer-based tools, largely Hewlett-Packard–developed, in its concurrent engineering. Their functions include schematic capture, printed-circuit layout, analog circuit simulation, three-dimensional mechanical design, and managing and transporting design files and materials lists.

> We called ourselves spider web teams: we caught all the defects in production and in the field and eliminated them

These tools are linked electronically to machine tools, board fabrication equipment, automatic component assembly machines, and board-level test equipment. All of them help us do our jobs more efficiently, though none of them is required for concurrent design. All that is required for CE is people working together.

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Case history 2: Cisco Systems

Ingredients for a booming start-up: collaboration, communications, consensus

Just another Silicon Valley start-up in 1984, Cisco Systems Inc. has undergone dramatic growth, much of it attributable to concurrent engineering (CE). Revenues jumped from US $27 million in 1989—when this approach was first adopted—to $70 million in 1990. In the first half of 1991 alone, the company logged sales of more than $76 million.

Robert W. Burnett Cisco Systems Inc.

Cisco makes multimedia and multiprotocol internetworking products: routers, bridges, terminal servers, and network managers for wide-area networks that link geographically dispersed local-area networks.

In the early days, the manufacturing department was never involved in the product design process. Only after the engineering department had delivered prototypes to a customer was the product handed off to manufacturing.

By 1989, it was clear that engineering's "toss it over the wall" practices could not continue. Problems were cropping up that were clearly caused by poor communication: a chip did not meet its specifications; yields were low on certain circuit boards; and field failures were cropping up.

At first, weekly review meetings were set up for engineering, manufacturing, and sales to address concerns like these. (Though the meetings were scheduled only when problems occurred, they were the genesis of CE at Cisco.) Good results were seen almost immediately.

Weekly review meetings helped cut the cost of a multiport communications interface (MCI) card providing up to two Ethernet connections and two serial connections. Even when an order called for only one or two interfaces, the MCI card was always stuffed with four because engineering had developed no way to test a less-than-fully-populated card. The cost of components and assembly was far higher than it had to be. Manufacturing therefore asked engineering to develop tests for cards with one to four interfaces, which was done.

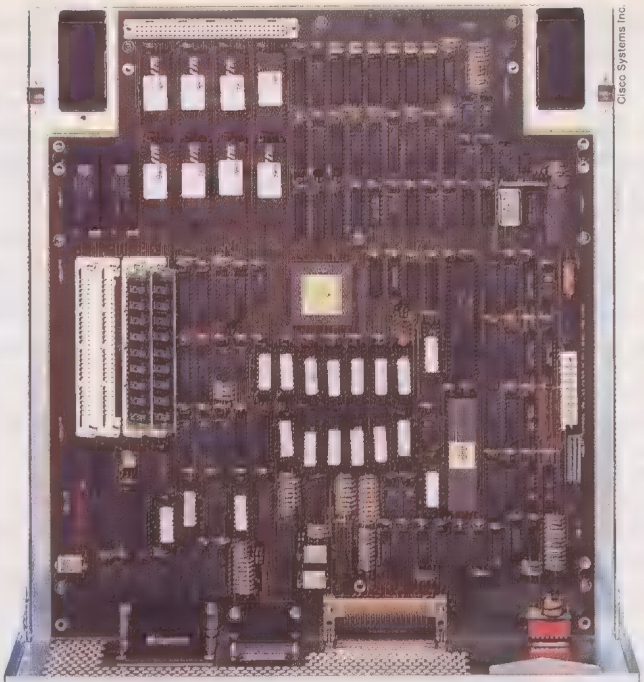
COSTS OUT OF HAND. Another headache was a serial communications chip on the MCI card. The chip sometimes produced an error when it handled odd-sized data packets. Costs got out of hand because the chip had to be ordered in extra-large quantities to ensure an adequate supply of good parts. Cisco engineering and manufacturing, through the weekly review meetings, worked with the vendor and a consultant to modify the chip until the problem was solved.

Then there was the manufacturing "bone pile"—the stack of circuit cards that had failed tests during manufacture. Engineering had created only meager diagnostic tests for these rejects. As a result, manufacturing could not find the cause of many of the failures and could not correct them—and the bone pile got bigger. At the weekly review meetings, engineering agreed to assign diagnostic programmers to manufacturing, and the two groups agreed to work together to select vendors in hope of securing better-qualified parts.

By late 1989, the groups had resolved to collaborate in true CE style to anticipate problems and avoid delays and bottlenecks.

Cisco at the time was designing its most complex product yet, a dual-bus internetwork router for a high-speed fiber distributed data interface (FDDI). But even though

Multiprotocol router and bridge was the manufacturer's first fully concurrently engineered product. The product team was able to shrink the electronics onto a single circuit board. Manufacturing joined in development from the time the unit was just a marketing idea.



Cisco Systems Inc.

development was well under way, manufacturing had not yet started to gear up to produce it—and it was very different in construction from earlier products. With the new cooperative relationship, manufacturing was to become involved at the prototype stage at the latest, well before any shipments to customers.

GOING TO BAT. However, the manufacturing group was traditionally understaffed at Cisco. Engineering took up manufacturing's cause and insisted that management hire the manufacturing talent needed.

For the first time, manufacturing engineers worked full time with hardware and software engineers; they helped to debug card designs and write diagnostic tests, for example. One manufacturing engineer even became a "star" by suggesting a way to make the unit much easier to manufacture and test. This experience convinced Cisco engineers that early cooperation paid dividends.

The first FDDI router was shipped to a customer on schedule in May 1990. The board test time was 40 minutes—it would have been at least 60 minutes without CE. The test time has since been reduced to 20 minutes.

Cisco's first opportunity to implement CE at the very beginning of a product's life came in December 1989, when work started on an integrated gateway server (IGS), the first product to shrink a router onto a single circuit board.

Manufacturing proposed ways to reduce the number of parts and suggested component types that would make the IGS easier to build and cheaper. For example, they suggested that the power subsystem be designed as a single unit to speed testing. They showed how the number of fasteners could be reduced by 70 percent. They drew from their experience to recommend against using certain parts that can be broken easily, even though they might be preferable from an engineering standpoint; for example, a connector that extended higher than other components on an earlier interface card had provoked customer complaints about breakage. And they made sure their colleagues from engineering understood the pitfalls of choosing components available from only one supplier. This was the first time that such issues were addressed at the outset, not after a design was finished and problems were already surfacing.

MYSTERY TOPICS. Today, Cisco still has its weekly review meetings. But now every new product at Cisco is guided by a team whose members come from many groups: hardware and software engineering, manufacturing, customer engineering, marketing, and business development. Each member is involved in every stage of the product cycle. Today, active engineering problems seldom arise; they are avoided by teamwork and forethought. The weekly team gatherings are more likely to review the team's progress and consider an occasional "mystery" topic—why, for example, does a power supply that works in the United States fail in Australia, even though its specifications were developed for both places.

ABOUT THE AUTHOR. Robert W. Burnett is vice president, engineering, at Cisco Systems Inc., Menlo Park, Calif. Before he joined Cisco in April 1989, he was program manager for digital branch exchanges at IBM Corp.'s Rolm subsidiary. He has a B.S. in psychology from Stanford University, California, and an MBA from Golden Gate University, San Francisco. ◆

Case history 3: Raytheon

Large-scale projects: developing Patriot missiles and other big systems

It was the mid-'80s when Raytheon Inc. began moving toward concurrent engineering (CE) in its Government Group, producer of such systems as the Patriot air defense missile system. The far-reaching CE environment, now serving about 400 workstations at the Lexington, Mass., headquarters and throughout New England, has resulted in many changes.

For the circuit designer, electrical performance is no longer of overriding interest. Rather, the goal is the best design in terms of total quality. By total quality is meant a balance of performance, ease of manufacture, and ease of support. The objectives of product assurance have done an about-turn, too—from inspection of the finished product to ensuring the quality of a design from the beginning. Doing it right the first time is now everyone's goal.

Raytheon divides its emerging CE environment into three parts [see figure]:

- System-level design, for planning the highest-level strategies to meet system performance objectives; the design is decomposed into subsystems, or modules, each with performance and supportability objectives.
- Module-level design, where the product is evolved in line with the goals assigned to it at the system level.
- System management level, which tracks design flow and monitors system design objectives.

System-level design will be done at a System Concept Station now under development. This is a workstation with a common user interface supporting four main functions: proposal management, system-level analysis, partitioning, and, in some cases, compilation of product specifications. The concept station must capture the project structure as defined in the statement of work about what's to be done, and link it to the design and module specifications.

For proposal management, the workstation must accept a statement of work either as a text file or by scanning printed pages. It should also supply tools for organizing requirements and for electronic lookup of key words and sections. New work requirements have to be matched with subsystems of previous projects and links established to retrieve pertinent past data, useful for tradeoff studies and preliminary costing.

This past data will be stored in a database alongside the system design data and information on not only why the original data was selected, but how and why it may have been reinterpreted. Similarly, new analytical results will be linked to the statement of work and a tally maintained of requirements that have been met.

SYSTEM-LEVEL ANALYSIS. Analyses are performed by a collection of programs being put under a common user interface. The framework is currently being architected to interface new programs with relative ease. As a rule of thumb, it should be possible to link a new program to the system in less time than it would take to train all the users in the program's original interface.

Raytheon uses life cycle cost modeling to estimate how much a system will cost the customer from concept through deployment and maintenance. Some of the life-cycle cost programs in use come from customers; others are developed in-house. The former include the General Electric Co. GE-Price model and the Navy FLEX 10 model. The GE model has served mostly to calibrate the database model. The FLEX model calculates design, production, and logistics-related costs for items like spares and training. The goal is to support why a particular design is best.

Cost models may start out as projections from experience with older systems. For example, if a new missile most resembles a Phoenix missile, then analogous parametric Phoenix costs become the basis for default data in the cost models. As new data is developed, it is inserted instead, improving the model's accuracy.

PARTITIONING. Partitioning a system breaks it down into a tree-like structure of successive sublevels, or subsystems, defining relationships between components. Design goals are assigned at each level of the hierarchy—for example, a reliability budget to ensure that the total systems reliability will meet the goal of the statement of work.

Several types of analysis are done to confirm that individual budgets are reasonable and that the overall systems objectives can be reached. The database captures the partitioned data, including the budgeted parameters, and stores where the requirements originated. The data is then annotated with scheduling and management data and placed under configuration control.

With the system definition complete, descriptions of what each subsystem must do are passed to individual designers. Writing this as a specification in English text runs into inherent ambiguities. So Raytheon is working with i-Logix Inc., Burlington, Mass., on expanding the formal modeling capabilities of that company's StateMate program for specifying a product's external behavior. The upshot is a combination of unambiguous state charts and functional flow and architectural diagrams whose performance can be simulated and compared to the system objectives.

> The principal interest of the circuit designer is no longer electrical performance—it is the best total quality

Raytheon and i-Logix have also been working together on perfecting the StateMate VHDL generator called Express VHDL. (VHDL stands for VHSIC hardware description language, VHSIC for very high-speed IC.) VHDL is used to define digital subsystem architecture and associated system test. Digital designers can then execute the VHDL specs and check if their implementation works.

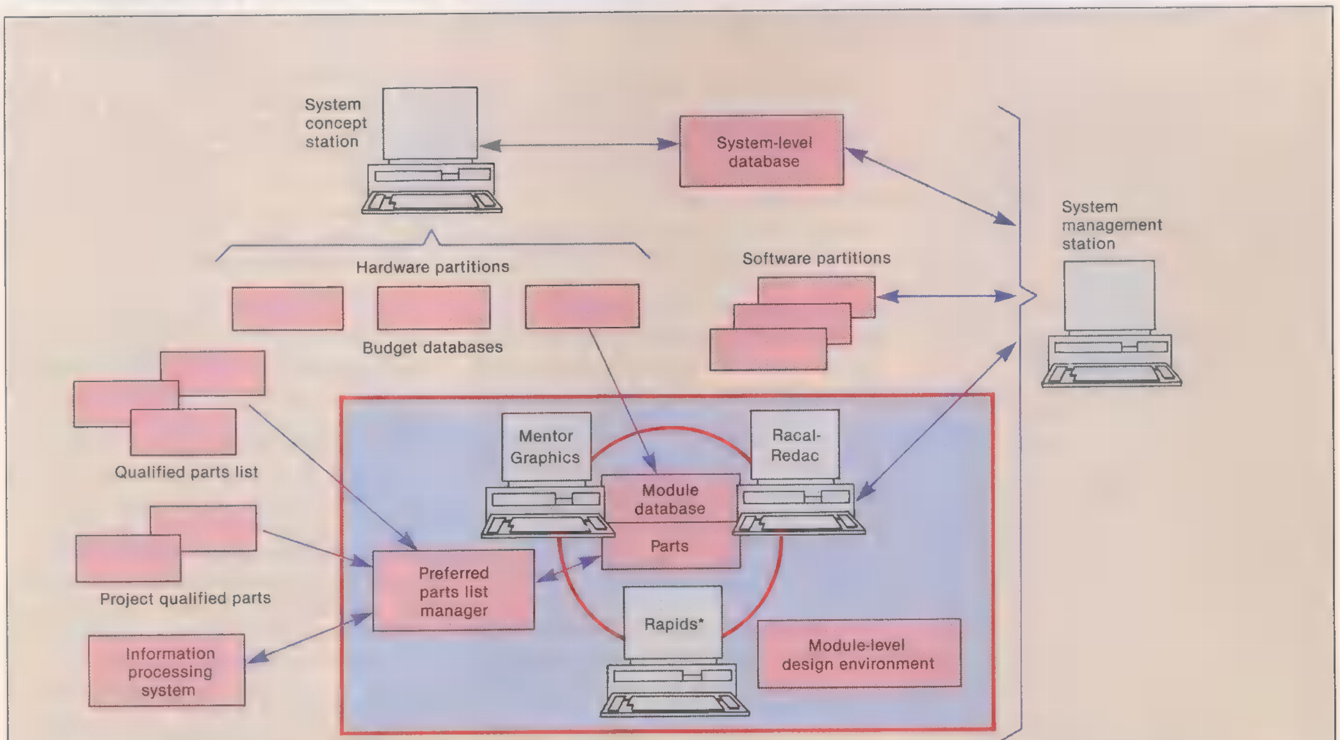
MODULE-LEVEL DESIGN. For the module-level design, Raytheon has an integrated set of printed-circuit board design/analysis tools under a common framework called Rapids (for Raytheon automated placement and interconnect design system). This system executes on the same Apollo/Hewlett-Packard platforms used for Raytheon's standard schematic/simulation system (from Mentor Graphics Corp., Beaverton, Ore.), and PC-board layout system (Visula from Racal-Redac Inc., Westford, Mass.).

The Rapids tool set mixes Raytheon proprietary and commercial programs to provide a CE environment for the designer. The system's appeal lies in its ability to develop logical approximations of design analysis data from parameters it obtains by analyzing the database.

For example, it can derive a very accurate estimate of the number of routing layers from only an initial netlist or a generic parts list along with physical features, including board boundaries. It can then use the estimate to show the designer how to improve manufacturing yield/cost drivers.

Commercial systems, in contrast, tend to insist on complete data sets. They can seldom estimate data that in a serial design approach is normally derived later. This distinction is critical: without this capability, it would be impossible to improve the design decisions that are made in the first 10 percent of the design cycle but determine up to 80 percent of the final cost.

OPTIMIZING MANUFACTURE. One major Rapids module fits components on boards and trades off the total number, size, and complexity of boards needed for a system against manufacturing cost and yield considerations. This module works with a rout-



*Raytheon automated placement and interconnect design system.

ing density analysis module to derive preliminary input for the Manufacturing Optimization Support System (MOSS).

MOSS's intent is to break the wasteful, recurring cycle of engineering change orders that result because of problems discovered during manufacture. For example, a design with small mounting pads may have poor yield because through-holes cannot be drilled accurately enough. Some holes may break the rim of the pad. However, enlarging the pads may further degrade yields if board density is so high that pad-to-line spacing causes shorts.

MOSS addresses such problems by establishing a model of the manufacturing process and its yield factors in relation to design parameters. MOSS checks out designs based on the very latest manufacturing parameters and design rules. It shares these with the system for estimating manufacturing costs and with a totally automated process control system. Linking these three systems with a common set of rules ensures that design analysis will always track the experience in the factory. MOSS also checks insertion machine clearances during component placement against the gripper sizes and shapes in the Raytheon factory that will build the part. This is a significant design-rule checking feature that is poorly supported in commercial layout systems.

Once the design is judged free of assembly errors, MOSS encourages design-for-manufacture tradeoffs. Both engineering- and manufacturing-related parameters can be varied to produce a spreadsheet list of product parameters versus cost and yield. There is also an expert system that can make suggestions for improving a design based on information captured from manufacturing experts.

Other analysis programs in Rapids feed back data to the designer as early in the design cycle as possible. One program handles thermal calculations that perform analyses much faster than a separate analysis team could. Although only approximations, these results are suitable for evaluating the quality of component placement. With the results immediately available, the board's thermal characteristics can have much more influence on where components are placed.

Another Rapids program conducts board-level reliability analyses based on Mil-HDBK-217 even before a board's thermal characteristics are fully known or linked to the placement thermal analysis. A third program performs critical signal analysis that automates the early detection of possible problems caused by path routes. The system can scan all paths, evaluating, say, stub lengths and the closeness of one signal to another, using rules customized for each class of signal on the board (that is, clock signal lines can have different rules than data buses). The signals can be assigned to classes during schematic capture and simulation, typically on systems from Mentor Graphics or Data I/O Corp., Redmond, Wash.

Rules for the classes can be obtained from a file shared by all boards on a project or modified for particular boards. These rules are translated to drive any of the automated routing systems used at Raytheon. Violations of the rules during routing are displayed graphically. Signals needing further study can be selected graphically on the screen, sent directly to Raytheon's version of Berkeley Spice for analysis, and the resulting graphs displayed on the screen.

SYSTEM MANAGEMENT ENVIRONMENT. Although defined as a separate system, the System Management Environment is really an extension of the System Level Design Environment and its System Concept Station. This module, currently at the concept specification stage, monitors schedules and design goal budgets set by the concept environment. It can also allow system-level design managers to make tradeoffs when individual modules fall short of their budgeted goals.

To do this, it manages the subsystem hierarchical tree generated during the system partitioning along with the design goal for each module. It allows the system-level manager to permit a particular module to exceed an assigned goal by determining at all levels of the system hierarchy if other modules can offset the problem. For example, if one type of module is consuming more power than budgeted, the system would automatically check to see if there was enough reserve power because other modules used less power than budgeted. ◆

> As a start, cost projections rely on data from older, similar missiles, updated as the design proceeds

Described by Jim Babish, Curtis Barton, and Joe Wong of the Missile Systems Division in Raytheon's Electronic Progress *magazine (January 1990, p. 26), Raytheon's concurrent engineering approach is updated in this article. —Alfred Rosenblatt*

Case history 4: ITEK Optical Systems

Making the one-of-a-kind type of product work right the first time

Even a company making one-of-a-kind items finds value in concurrent engineering (CE). This is the case at ITEK Optical Systems, a division of Litton Systems Inc. in Lexington, Mass., making high-tech optical and electro-optical products. The R&D company is an outgrowth of Boston University's Physical Research Laboratory. In the '70s it was building such systems as the cameras for the Viking Lander on Mars.

Currently, Itek is under contract to the California Association for Research in Astronomy and is developing and producing the primary mirror segments for the world's largest astronomical telescope at the W.M. Keck Observatory in Hawaii. This key project—producing 36 hexagonal glass segments, each 1200 pounds in weight and 1.8 meters across, for the 10-meter-diameter mirror—represents a big production run for Itek and several years' work, pointed out Fausto E. Molinet, assistant director for total quality management.

Itek's adoption of total quality management and concurrent engineering was part of a move Litton made in its divisions about three years ago to create an atmosphere of change and to improve operations.

"Many believed that process improvements developed with CE are of greatest benefit to high-volume manufacturers," said Molinet. "At first we thought that CE didn't apply to us because we would all be retired by the time we could figure out how to improve our processes."

But because Itek gets only one chance at making its products, it knew its processes should be improved. "We're in big trouble if we break a very expensive piece of glass while we're tooling it," said Molinet. "We must make sure that doesn't happen."

Itek decided to try CE by focusing on the teamwork aspects of design. The company began by involving many disciplines in the early stages of the design process.

At design management reviews the kinds of functions represented were expanded. "Before, an engineer doing a mechanical design may only have had the program and configuration managers and head of drafting at a design review," said Molinet. "Now we'll have a thermal designer and a contamination guy there, too."

The teams also found many more things to consider earlier in the design phase. Additional people were brought in whose expertise had only secondary or tertiary influence. The yardstick became that whatever had to be considered for manufacture had to be reflected in decisions made during design.

The company also set up careful reviews of all aspects of its design and manufacturing process, including the operational readiness of the machinery to be used. The readiness reviews were critical to ensuring that a tool, for example, would not push down an extra eighth of an inch and break the glass.

Once selected, the people on a project team cover lots of ground—from mechanical engineering to glass machining, from thermal analysis, drafting, and configuration management to software engineering,

Alfred Rosenblatt Managing Editor

ITEK Optical Systems Division, Litton Systems Inc.

The design and manufacture of products like this 50-kg, 1.5-meter-diameter flat mirror made of fused silica relies on a concurrent engineering approach taken by ITEK Optical Systems. The rib structure is visible because the reflective aluminum coating has not yet been applied. The need to balance strength, rigidity, and light weight requires a strong interaction between design and manufacturing functions.

designing programs for numerically controlled machines, and marketing. "Our object is to break down the barriers between the functions," said Molinet. "We all look at what we're doing as a continuous process, with each function providing inputs and lots of feedback loops."

When some people are not working on a major project, they work together on multifunctional teams to tackle problems associated with some facet of the business. Included are such areas as publications, security, and administration. Regular meetings are also held with top management. Though the teams try to change things themselves, they occasionally need a blessing from the top. That blessing may also come with a check for such things as a new computer.

PAYBACKS. One major team effort focused on the design-and-build documentation handed off to manufacturing, according to Molinet. The team explored what it could do to improve the process. First it looked at historical data: engineering change orders were counted and studied to decide what caused any difficulties. Was it a lack of information or did a supplier fail to deliver what was promised? The goals: fewer change orders, fewer rejects, and less rework.

"Also, by exchanging ideas, and in the process describing their own functions better, we created a new level of understanding among the people on the team," said Molinet. "Each person took this understanding back to [his or her] functional groups, and things they knew to be good started happening."

For instance, Molinet recalled how the maintenance people found they needed to know more about a new building's construction so they could do a better job of cleaning. Less dust and dirt was left to get into the tooling and scratch the glass.

But Itek also realized that the transfer of "good things" through the company was done largely by osmosis. It was necessary for that transfer to be accomplished on a more formal basis. Thus, work is now under way on a training program for many functions—designers, draftsmen, engineers, program managers, and manufacturing and maintenance personnel.

FAST TEAM RAMP-UP. After about 1½ years, Itek had only four teams considering general business problems. But once the company realized what the teams were accomplishing, that number was ramped up rapidly to 23 in the last year or so. The teams represent a third of the 500 employees.

Teams should include at least five people, noted Molinet. Otherwise, there may not be a quorum at meetings and "one or two people could drive the result, which we don't want," he said.

This year Molinet hopes to develop quantitative measures of the teams' successes. Those would be useful to management, he continued, but they would also help show the people involved that they are on the right track.

Right now, the feeling is that things are being done better with CE. Some activities—like putting a reflective coating on a new glass shape—are wrapped up on the first pass and "we couldn't do that before," said Molinet. "We can't always point to specific reasons for this. It could be the result of our reviews, or the care taken by the person doing the work, or a better design effort." But the results have already polished up the bottom line. "Productivity has improved dramatically," he said. ◆

TO PROBE FURTHER

Author Sammy G. Shina expands his introduction to concurrent engineering in his book *Concurrent Engineering and DFM for Electronic Products* (Van Nostrand Reinhold, New York, 1991). Author Jon Turino covers both management and technical aspects of the subject in *Concurrent Engineering* (Logical Solutions Technology, Campbell, Calif., 1991). Turino's book *Design for Test* (Van Nostrand Reinhold, 1990) provides guidelines for testability and includes information on software and documentation requirements.

IEEE Spectrum's editors review methods from around the world on how to shorten time to market in "Managing to be competitive in a global context," a special issue on research and development, October 1990.

In *Design for Manufacturability* (CIM Press, Lafayette, Calif., 1990), David M. Anderson offers guidelines for designers in a concurrent engineering environment. William G. Beazley, in *The Contractor's Guide to CALS and Concurrent Engineering* (Pasha Publications, Arlington, Va., 1991), answers questions about compliance with the Department of Defense's computer-aided acquisition and logistics support (CALS) requirements.

IEEE Design and Test of Computers Magazine published a special issue on concurrent engineering in March. For copies, call 800-272-6657. *Computer Design News* presents monthly case histories of successful implementations. For more information about these articles, call 508-692-0525.

The Institute for Defense Analyses, Alexandria, Va., documented its landmark study for the U.S. Department of Defense in "The Role of Concurrent Engineering in Weapons Systems Acquisition" (IDA report R-338, 1988). Contact the institute at 703-325-9634.

For subscriptions to CERCnet, the Concurrent Engineering Research Center's electronic information repository, contact the center at Drawer 2000, West Virginia University, Morgantown, W. Va. 26506; 302-293-7226; e-mail, jrs@cerc.wvu.wvnet.edu. *CERC Outlook*, a bimonthly newsletter that details current activities, is available from the same address. CERC cosponsored the Third National Symposium on Concurrent Engineering, June 10–14, in Washington, D.C.

The books by Ishikawa and Taguchi remain among the best sources of information about their methods: *Guide to Quality Control*, by Kaoru Ishikawa (1982), and *Introduction to Quality Engineering*, by Genichi Taguchi (1986). Published by the Asian Productivity Organization, both are available from Quality Resources, White Plains, N.Y. 10601; 914-761-9600.

The Harvard Business Review recently published overviews of two key design-optimization methods: "The House of Quality" by John R. Hauser and Don Clausing, May-June 1988, reprint 88307, and "Robust Quality" by Genichi Taguchi and Don Clausing, January-February 1990, reprint 90114. Both are introductory treatments for management, and contain example applications. For copies, call 617-495-6800.

Selecting math coprocessors

Hardware and software compatibility, accuracy, and power consumption should be considered along with price and performance

Today's personal computers are built with central processing units (CPUs) that typically provide hardware support for only integer arithmetic. How then do PC-based applications such as spreadsheet packages carry out computations involving real, or floating-point, numbers? One solution is to include in every application some software subroutines for performing addition and other common operations on floating-point numbers. A speedier alternative is to equip the PC with a math coprocessor, which extends the architecture of the CPU by supplying hardware support for floating-point arithmetic.

Most math coprocessors are optional peripherals that are installed inside the PC. However, there is more to using one than simply plugging it into the computer. The would-be buyer of any math coprocessor should first answer the questions: is it compatible with the CPU? Is there an appropriate socket in the computer for the math coprocessor? Is it approved for use with an application by the software vendor?

The focus here is on math coprocessors for the Intel 80386 (386) CPUs found in IBM-compatible PCs and the Motorola 68030 (030) CPUs found in Apple Macintosh II PCs. (But note that the most recent products from Intel Corp., Santa Clara, Calif., the i486, and Motorola Inc., Schaumburg, Ill., the 68040, integrate the CPU and the math coprocessor on one and the same chip.)

COMPUTER ARITHMETIC. Consider a program that uses the amortization formula to compute the size of the payment needed to amortize a loan by equal periodic amounts at a given interest rate per period. How does this program run on 386- or 030-based computers with hardware support only for integer arithmetic?

One technique, known as fixed-point arithmetic, represents each real number by a single integer. Using this technique, a programmer multiplies each piece of input data, intermediate result, and output data by scale factors so that they can be approximated by "reasonable" integers. "Reasonable" refers to the fact that the 386 and 030 CPUs provide hardware-supported integer arithmetic for numbers to 4 294 967 295 only—that is, 32-bit binary integers.

For use by homeowners, an appropriate scaling might be to measure dollar values as integer multiples of a penny, periods as integer multiples of months, and interest rates as integer multiples of 1 percent per year. For use by the Federal government, a suitable scaling might be to measure dollar values, periods, and interest rates in integer multiples of US $1000, days, and 0.01 percent per day, respectively. Every time the scaling of the parameters changes, however, the formula used to compute the payment changes, and so does the program derived from the formula.

To avoid constantly rewriting programs, programmers have turned to floating-point arithmetic, in which the scaling is incorporated not into the formula, but rather into the numbers that appear in the formula.

Math coprocessors enable personal computers to run simulation, design, and data analysis packages used by engineers and scientists

Many textbooks in computer science describe the floating-point representation of numbers (as values between 1 and 10, times a power of 10) and present algorithms that use a CPU's shift and integer arithmetic instructions to carry out floating-point arithmetic. A math coprocessor speeds this kind of computation by implementing in hardware the algorithms that carry out floating-point arithmetic.

The introduction of math coprocessors enabled PCs to effectively run floating-point–intensive applications. These applications include simulation, design, and data analysis packages used by scientists and engineers, as well as two of the most common PC-based applications, spreadsheets and desktop publishing.

Heavy use of a math coprocessor occurs when a spreadsheet carries out WHAT-IF analyses. Such analyses usually correspond to optimization problems that are solved by algorithms that repetitively carry out a particular sequence of floating-point operations.

Desktop publishing applications often use page description languages (PDLs) to describe their output. Many PDLs, like PostScript from Adobe Systems Inc., Mountain View, Calif., are sophisticated graphical applications tailored to the description of printed or displayed text and graphics. Like many graphical applications, PDLs use mathematically defined line segments and arcs to form text characters and other graphic images. A math coprocessor speeds the mathematical calculations that determine which pixels on the screen, or which dots on the printer, should be used to depict line segments and arcs. For example, Custom Applications Inc., Billerica, Mass., markets a package, called Freedom of Press, which allows PostScript output to be produced on non-PostScript output devices. A math coprocessor typically speeds Freedom of Press execution by 25–150 percent.

MORE USES. Math coprocessors are required by many PC-based applications used by scientists and engineers. These packages include AutoCAD, a popular computer-aided design package marketed by Autodesk Inc., Sausalito, Calif., and Prime Factor FFT, a digital signal analysis package sold by Alligator Technologies Inc., Fountain Valley, Calif.

3D Studio, a multimedia application marketed by Autodesk, allows users to create and render three-dimensional models of a scene. The goal of the rendering process is to produce an image of the scene comparable to a photograph in quality. Properly accounting for the sources of light, casting of shadows, surface textures and reflection or transmission properties of the objects in the scene is a very computationally intensive task that becomes feasible on a PC only when the machine is equipped with a math coprocessor.

Warren E. Ferguson Jr. Cyrix Corp.

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Digital ChoreoGraphics

A math coprocessor helps draw the space shuttle in proper perspective and lighting in one-third the time of a software emulation.

There are two basic types of math coprocessors available today: standard and memory-mapped.

The standard type seamlessly augments the functionality of the CPU. First, floating-point instructions for standard math coprocessors are included among the instructions recognized by the CPU. Second, when the CPU recognizes a floating-point instruction in its instruction stream, it can decide whether a standard math coprocessor or an emulator is to be used to execute the instruction.

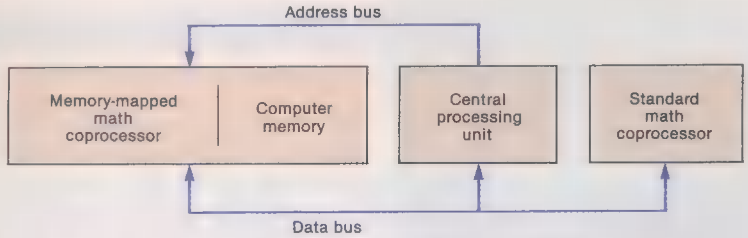
How can the 386 make this decision? The 386 has an emulate (EM) bit that indicates whether or not a standard math coprocessor is installed. If the EM bit is clear, indicating that a standard math coprocessor is installed, the 386 sends any floating-point instruction it encounters to the coprocessor for execution. If the EM bit is set, which indicates that a standard math coprocessor is not installed, then the 386 generates a coprocessor-not-available exception when it encounters a floating-point instruction.

The occurrence of this exception forces the 386 to pause execution of the program that contains the floating-point instruction and to switch control to an exception handler. This exception handler is simply an emulator whose task is to compute, using non-floating-point instructions, the result that would have been returned by a standard math coprocessor. After the exception handler finishes its task, execution of the program is resumed at the point immediately following the floating-point instruction that

Characteristics of representative math coprocessors

Math coprocessor	Compatible CPU	Type	Power, mW	List price, speed	Data formats[2]	Clock cycles, typical or min-max range[3]						
						Add	Mult	Div	Tan	Atan	Exp	Log
Cyrix 83S87	Intel 386SX	Std.	350 typ.	US $556 20 MHz	S,D,DE	15	19	27	75	83	63	87
Cyrix 83D87	Intel 386DX	Std.	500 typ.	$994 33 MHz	S,D,DE	15	19	27	75	83	63	87
Cyrix EMC87	Intel 386DX	Std. and MM[1]	500 typ.	$994 33 MHz	S,D,DE	6	10	19	75	83	63	87
Intel 8087	Intel 8086/8088	Std.	2375 max.	$142 5 MHz	S,D,DE	70–100	90–145	193–203	30–540	250–800	310–630	700–1000
Intel 80287XL	Intel 80286	Std.	675 max.	$326 12.5 MHz	S,D,DE	30–38	25–53	95	198–504	321–494	215–483	264–554
Intel 387SX	Intel 386SX	Std.	1000 typ.	$550 20 MHz	S,D,DE	23–31	29–57	88	191–497	314–487	211–476	257–547
Intel 387DX	Intel 386DX	Std.	750 typ.	$994 33 MHz	S,D,DE	12–26	17–50	77–80	162–430	250–420	167–410	210–447
Intel i486	Intel i486	Std.	4500 max.	$667 33 MHz	S,D,DE	8–20	16	73	200–273	218–303	140–279	171–326
Motorola 68881	Motorola 68020/68030	Std.	750 max.	$68 20 MHz	S,D,DE	51	71	103	473	403	545	571
Motorola 68882[4]	Motorola 68020/68030	Std.	750 max.	$218 40 MHz	S,D,DE	56	76	108	476	406	548	574
Weitek 3167	Intel 386DX	MM	2363 max.	$995 33 MHz	S,D	6,6	6,10	38,66	340, SEM[5]	298, SEM	401, SEM	365, SEM
Weitek 4167	Intel i486	MM	1838 max.	$1295 33 MHz	S,D	2,2	3,3	17,31	N.A.[6]	N.A.	N.A.	N.A.

1 MM = memory-mapped.
2 S = single-precision; D = double-precision; DE = double-precision extended (all compatible with IEEE Standard 754).
3 For S and D formats for Weitek; otherwise for DE format.
4 Can execute up to two floating-point instructions simultaneously.
5 SEM = software emulation (supplied by Weitek).
6 N.A. = not available.



The floating-point instruction and data are received from the CPU sequentially by standard math coprocessors but in parallel by the memory-mapped coprocessors. In the first case, only the data bus is used; in the second, the address bus is used to transmit the instruction. Many 386-based PCs allow either a standard or memory-mapped math coprocessor to be installed.

caused the exception.

The 030 handles this situation a little differently. It sends all floating-point instructions to the coprocessor socket. If it does not receive an acknowledgment that an instruction was received, then the 030 generates an exception. This is resolved by an exception handler just as it would be by a 386-based PC.

MEMORY-MAPPED. A memory-mapped coprocessor assigns a unique memory address to each floating-point instruction. For example, address 1948 might correspond to one that adds a floating-point number to the contents of the coprocessor's register 1. Then, whenever the coprocessor sees data being written to address 1948, it knows that it is being asked to take the number simultaneously present on the data bus and add it to the contents of the coprocessor's register 1.

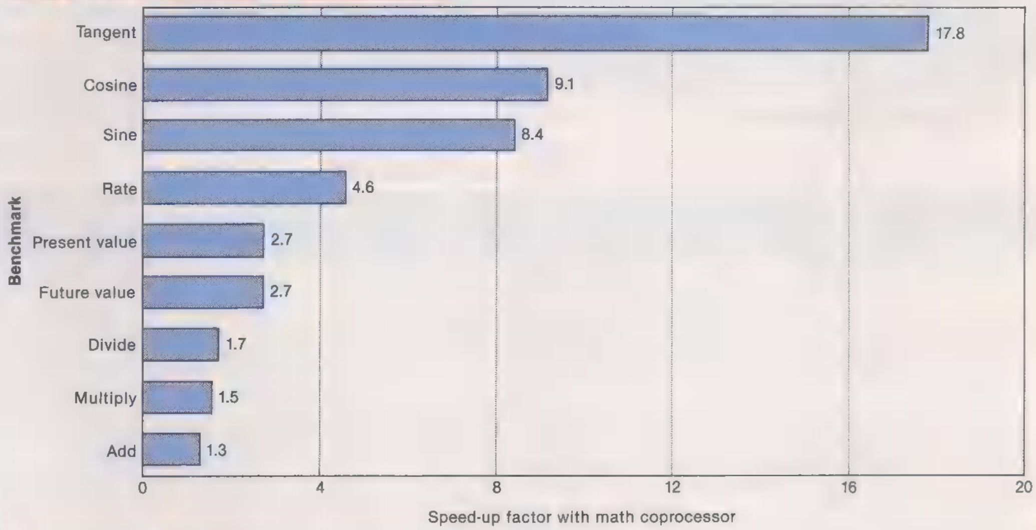
The 386 does not differentiate between addresses associated with memory and those associated with a memory-mapped math coprocessor. Consequently, the latter is seldom considered a seamless extension of the 386's architecture.

Recall that the status of a 386's EM bit indicates whether or not a standard math coprocessor is installed. Unfortunately, the 386 does not contain a bit that records whether or not a memory-mapped coprocessor is installed. This fact makes it more difficult to write applications that either use a memory-mapped math coprocessor when installed or emulate one when not installed.

COMPARISONS. Memory-mapped math coprocessors are rarely available for use with 030-based PCs. But for 386-based PCs, compatible standard and high-performance memory-mapped math coprocessors are available.

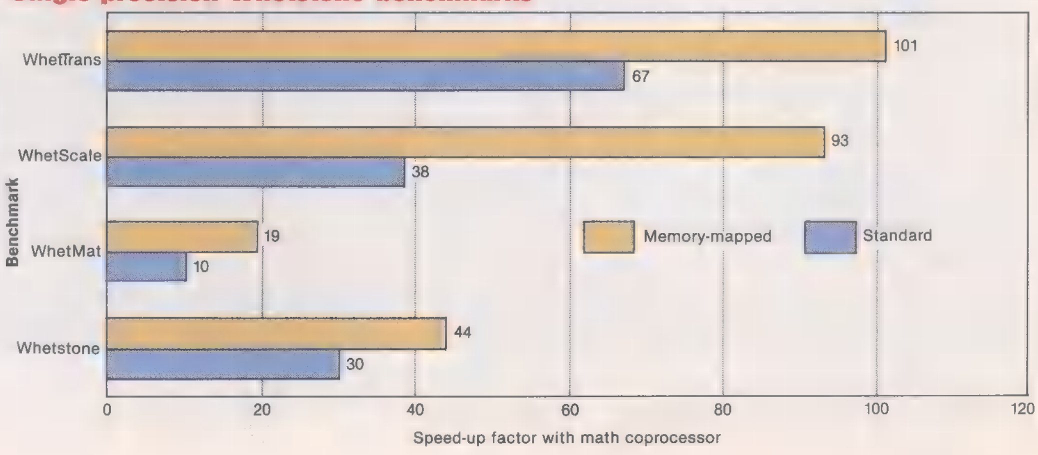
A simple means of measuring the performance of math coprocessors is to compare how many clock cycles each instruction takes to execute. For example, the Cyrix EMC87 adds two floating-point numbers in 15 clock cycles when used as a standard math coprocessor, and in six clocks when used as a memory-mapped one. One reason for this difference is that standard math coprocessors must be fully synchronized with the CPU, and this synchronization consumes clocks not related to the execution of floating-point operations. A second reason is that the CPU passes instructions and data to standard math coprocessors sequentially, but to memory-mapped math coprocessors in parallel—and therefore faster.

Lotus 1-2-3 Release 3 benchmarks



Cyrix Corp.'s Lotus 1-2-3 Release 3 benchmarks are spreadsheets that consist of a 52-by-50 matrix of cells, each filled with a formula for the operation indicated. Speed-up factors with standard math coprocessors are indicated.

Single-precision Whetstone benchmarks



NDP Fortran single-precision Whetstone benchmarks from MicroWay Inc., Kingston, Mass., running on a 386-based PC, indicate the degrees to which the addition of a standard or memory-mapped coprocessor speeds computation.

Another feature that distinguishes one math coprocessor from another is the programming model they offer programmers. Such a model includes the floating-point instructions executed by the coprocessor, the data types it recognizes, and the number and functionality of its registers. Standard math coprocessors for Intel-based PCs offer similar, but not identical, programming models to their users. For example, the Intel 8087 coprocessor does not recognize the Intel 387DX coprocessor's instruction for computing the trigonometric sine.

Memory-mapped math coprocessors for 386-based PCs can offer very different programming models to their users. For example, the instruction set and register functionality of the 3167 from Weitek Corp., Sunnyvale, Calif., differs significantly from that of standard math coprocessors.

The EMC87 from Cyrix Corp., Richardson, Texas, however, offers functionally equivalent programming models when used as either a standard or a memory-mapped math coprocessor. Most applications written in Microsoft C, Fortran, Borland Turbo C, or Turbo C++ use only standard math coprocessors. By means of the code translator provided with the EMC87, however, it is possible to substitute for each standard floating-point instruction its EMC87 memory-mapped equivalent.

IEEE 754. Standards encourage competition in any field, and math coprocessors are no exception. In 1985 the IEEE Floating-Point Working Group published its standard, called the ANSI/IEEE Standard 754-1985, for binary floating-point arithmetic. Over 90 people participated in the group, and their deliberations extended over seven years.

The group's combined experience led its members to consider how to eliminate or at least minimize many of the bad properties found in prior implementations of floating-point arithmetic. For example, manufacturers often used proprietary formats to store floating-point numbers and did not always return the correctly rounded result of common operations like addition or multiplication. The IEEE 754 Standard accordingly describes a programming environment that explicitly defines:

- How floating-point numbers should be stored within the computer.
- How floating-point numbers should be combined through the common operations of addition, subtraction, multiplication, and division.
- What types of errors should be reported, and how they should be reported, to the application and its user.

Should users care if their math coprocessor adheres to the IEEE 754 Standard? Many of the popular PC-based applications, like those developed by Microsoft Corp., Lotus Development Corp., and Borland International Inc., have been designed around the standard. These vendors find that a goodly portion of their customer support involves answering questions about floating-point arithmetic. This expense is reduced if a coprocessor adheres to the standard. First, these vendors can use properties of the standard to design algorithms that are robust and that perform in a predictable and mathematically precise manner. Second, if both the customer's and the vendor's coprocessors conform to the same standard, then it is easier for the vendor to reproduce any problems encountered by its customers.

CHOOSING MS. RIGHT. Price and performance of course merit consideration in choosing a math coprocessor. But hardware compatibility, software compatibility, accuracy, and power consumption should not be overlooked.

Hardware compatibility requires the math coprocessor to be compatible with the CPU. Furthermore, the PC must have a socket for the math coprocessor. Most 386 desktop PCs have a 121-pin socket that accepts either the standard or the memory-mapped variety. Many 386 laptop PCs, however, have a 68-pin coprocessor socket that accepts only the standard kind. Finally, all Apple Macintosh II PCs, except the Apple Macintosh IIsi, have factory-installed math coprocessors.

> Power consumption is important because heat shortens the life of both the math coprocessor and the PC it is installed in

Software compatibility involves many issues. What types of math coprocessors can be used with the desired software application—only standard math coprocessors or the memory-mapped type? What functionality does the software application assume the math coprocessor to possess? The vast majority of floating-point applications for IBM-compatible PCs assume that standard math coprocessors are functionally compatible with Intel's 387DX—that is, they can recognize and correctly carry out all 387DX-style floating-point instructions.

Accuracy considerations play a role when the math coprocessor carries out a lengthy computation. Most applications, including those developed with common high-level languages, use IEEE 754 Standard double-extended precision floating-point arithmetic to limit the growth of error during a computation. For example, applications written in Microsoft's Fortran or C or Borland's Turbo Pascal or Turbo C employ double-extended precision arithmetic as the default precision of numbers stored in the math coprocessor's registers. IEEE 754 Standard double-extended precision floating-point arithmetic is available on most, but not all, math coprocessors.

Power consumption is important because heat shortens the lifetime of both the math coprocessor and the PC in which it is installed. For battery-operated laptops, power consumed by the math coprocessor also affects how often its battery will need recharging.

TO PROBE FURTHER. "Math Coprocessors" by L. Brett Glass, *Byte*, January 1990, pp. 337–48, describes in more detail the programming models provided by standard math coprocessors used with the Intel 80386 and Motorola 68030. "Macintosh Numerics: An Environment for Scientific Computing" by Ali Sazegari, *Computers in Physics*, July/August 1990, pp. 355–57, describes the SANE environment found on all Apple Macintosh PCs.

The implementation in software of floating-point arithmetic, via shift and integer arithmetic instructions, can be found in *The Art of Computer Programming, Volume 2: Seminumerical Algorithms* by Donald Knuth (Addison-Wesley, 1981, second edition). Copies of the IEEE 754 Standard can be obtained from Customer Service at the IEEE Standards Department, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331; 908-562-3820.

Jerome T. Coonen's 1984 Ph. D. thesis for the University of California-Berkeley, titled "Contributions to a Proposed Standard for Binary Floating-Point Arithmetic," contains many interesting topics related to his participation in the IEEE 754 working group. Cyrix Corp. has ported one of his programs, called FPTEST, to 386-based PCs so that users can test the compliance of Intel 387-compatible standard math coprocessors with the IEEE 754 Standard. For a free copy of this disk contact Cyrix Corp., Box 850118, Richardson, Texas 75085-0118, Attn: IEEE Test Vectors.

ABOUT THE AUTHOR. Warren E. Ferguson Jr. joined Cyrix Corp., Richardson, Texas, as a senior algorithms designer in June 1990. Prior to that, he was a consultant to Cyrix and helped develop the algorithms used to compute the transcendental functions found in Cyrix's FasMath line of math coprocessors. Ferguson was an assistant professor of mathematics at the University of Arizona, Tucson, and an associate and full professor of mathematics at Southern Methodist University, Dallas. He earned his B.S. in physics from Clarkson University, Potsdam, N.Y., in 1971, and his Ph.D. in applied mathematics from the California Institute of Technology, Pasadena, in 1975.

1991 Major Medalists

The IEEE honors 12 outstanding contributors

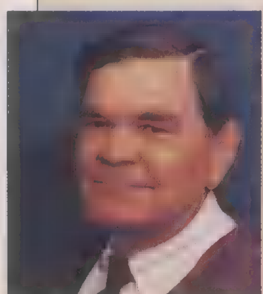
IEEE Medal of Honor
Leo Esaki

Leo Esaki (F), an IBM Fellow at the Thomas J. Watson Research Center, Yorktown Heights, N.Y., is the recipient of the 1991 Medal of Honor "for contributions to and leadership in tunneling, semiconductor superlattices, and quantum wells." The award, as well as the IEEE major medals to 11 honorees, were scheduled to have been presented on June 16 in San Francisco.

Esaki attended the Third High School in Kyoto, Japan, and majored in physics at the University of Tokyo. He joined Sony Corp., where he discovered the first quantum electronic device, the tunnel diode, in 1957. That work also earned him a Ph.D. in physics and the 1973 Nobel Prize in physics.

In 1960 Esaki joined the Thomas J. Watson Research Center. Much of his research work there has centered on man-made semiconductor structures such as superlattices and quantum wells. Many electron-transport and optoelectric devices have been based on the discoveries made in this field.

Esaki visits his homeland regularly and serves as a director of IBM-Japan and the Yamada Science Foundation. He is also a member of the Japan Academy and an adjunct professor of Waseda University.



IEEE Edison Medal
John L. Moll

John L. Moll (LF), associate director of the Superconductivity Laboratory, Hewlett-Packard Laboratories, Palo Alto, Calif., has been awarded the Edison Medal "for pioneering contributions to diffused and oxide-masked silicon devices, transistor analysis, the p-n-p-n switch, and optoelectronics."

As a result of Moll's work at Bell Telephone Laboratories from 1952 to 1958, silicon was identified as the most appropriate available semiconductor technology. That breakthrough evolved into the Ebers-Moll transistor model as well as the theory for the p-n-p-n switch. Moll taught electrical engineering at Stanford University in California from 1958 to 1970, worked on the development of optoelectronic devices at Fairchild Camera and Instrument Co. from 1970 to 1974, and since 1974 has worked on bipolar and MOS devices and superconductor materials and devices at Hewlett-Packard.

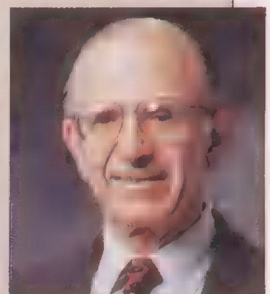
IEEE Lamme Medal
Shotaro Tominaga

Shotaro Tominaga (F), president, Ryokoh Computer Systems Co., Hommachi Amagasaki City, Japan, is the recipient of the Lamme Medal "for contributions to the development of SF_6 gas circuit breakers, zinc oxide surge arresters, and gas insulated switchgear and substations."

Tominago joined Mitsubishi Electric Corp., Amagasaki City, Japan, in 1950, and worked there in various capacities until 1983, when he was appointed manager of the Engineering, Energy, and Industrial Systems Group in Tokyo. He concurrently served as general manager of the Mitsubishi Fusion Center. In 1988 he joined Ryokoh Computer Systems, a Mitsubishi Electric Group company, and a year later became president of the firm.

As a result of his contributions, the first commercial 500-kV hybrid gas-insulated switchgear (GIS) was installed in 1973 and the first 500-kV full GIS, in 1976.

IEEE Founders Medal
Irwin Dorros



Irwin Dorros (F), executive vice president–technical services, Bell Communications Research (Bellcore), Livingston, N.J., has won the Founders Medal "for distinguished technical leadership in the evolution of national telecommunications networks and the implementation of a major R&D resource."

Dorros began his professional career with Bell Telephone Laboratories in 1956. His work there included development of electronic switching, data communications, and pulse-code-modulation digital transmission systems, as well as cellular radio and the Picturephone. In 1978 he joined AT&T Co. as assistant vice president–network planning with responsibility for leading the planning of the evolution of the then Bell System nationwide network. He was also a technical leader for AT&T's defense in the proceedings leading to the breakup. He was named to his present position in 1982 and has directed the creation of Bellcore's technical services area.

IEEE Education Medal
Hermann Anton Haus

Hermann Anton Haus (LF), Institute Professor of the Massachusetts of Technology (MIT) in Cambridge, is the recipient of the Education Medal "for creative contributions to education in electromagnetic fields and waves, and quantum electronics."

With the exception of brief interruptions, Haus has been at MIT since he obtained a Sc.D. there in 1954. He became a full professor in 1962, was given the Elihu Thomson chair in 1973, and was made an Institute Professor in 1986. His teaching has concentrated on electromagnetic field theory, microwaves, and optoelectronics, while his research has centered on noise in microwave tubes, lasers, quantum noise, and short pulse generation with lasers.

Haus has authored and coauthored two books on noise and over 180 journal articles, and holds five patents, one of which is a shared patent for the quarter-wave shifted distributed feedback laser.

IEEE Simon Ramo Medal
Paul E. Green Jr.

Paul E. Green Jr., manager, advanced optical networking, IBM Corp., Thomas J. Watson Research Center, Yorktown Heights, N.Y., is the recipient of the Simon Ramo Medal "for the introduction of modern system techniques to the interpretation of seismic waves, and the application of these techniques to distinguishing earthquakes from underground nuclear explosions."

Green's doctorate thesis on correlation detection of stored signals at the Massachusetts Institute of Technology (MIT) led to the first operational spread-spectrum system. While at MIT's Lincoln Laboratory from 1951 to 1969, he and his group worked on extending communication concepts to a new kind of communication channel—one lying between a seismic receiving system and a distant source that can be either an earthquake or an underground explosion. Since 1969, he has been at IBM, where he is manager of advanced optical networking.

IEEE Medal for Engineering Excellence
Alexander Feiner

Alexander Feiner (F), executive director, Integrated Systems Division, AT&T Bell Laboratories, Middletown, N.J., has been awarded the Medal for Engineering Excellence "for exceptional contributions to system architecture, methodology, and design of modern digital PBXs."

When Feiner began working at Bell Laboratories in 1953, he joined with others in investigating the application of electronic techniques to telephone switching. In 1959 he proposed a new type of electromagnetic device, the ferreed, as well as a new network topology for the switching network based on that device. He was promoted to department head, directing the development of the hardware for the No. 1 switching system.

In 1969 Feiner became a director of a laboratory concerned with technology used in customer premises switching. He assumed his present position in 1983.

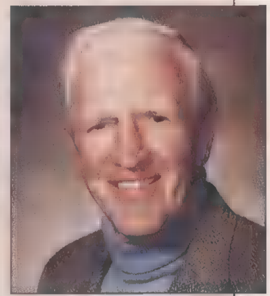
IEEE Richard W. Hamming Medal
Elwyn Berlekamp

Elwyn Berlekamp (F), president of Axcom Inc., Berkeley, Calif., and professor both of electrical engineering and computer science and of mathematics at the University of California, Berkeley, has won the Richard W. Hamming Medal "for profound contributions to the theory and application of error-correcting codes."

After five years at Bell Telephone Laboratories, Berlekamp received his present professorships at the University of California in 1971. In 1982 he started teaching part-time in order to pursue industrial research and engineering at Cyclotomics, a company he founded, which later became a subsidiary of Eastman Kodak Co.

From 1967 through the late 1980s Berlekamp and his colleagues introduced a series of major improvements in algorithms for decoding sophisticated algebraic codes, especially Reed-Solomon codes. He has patented 12 inventions and has authored over 75 articles.

IEEE Alexander Graham Bell Medal
C. Chapin Cutler



C. Chapin Cutler (LF), a former professor in the department of applied physics at Stanford University in California, and now retired, is one of three recipients of the Alexander Graham Bell Medal "for the invention and development of predictive coding of pictures and picture sequences."

Cutler was engaged in research at Bell Telephone Laboratories from 1937 until 1979, when he joined Stanford University. Holding 80 patents, he was an early contributor to the development of wideband microwave amplifiers.

IEEE Alexander Graham Bell Medal
John Ormond Limb

John Ormond Limb (F), laboratory manager, Hewlett-Packard Co., Cupertino, Calif., is a second recipient of the Alexander Graham Bell Medal.

Limb joined Bell Laboratories, Holmdel, N.J., in 1971, where he worked on the coding of picture signals to reduce channel capacity requirements, and on developing office information systems and local-area networks. In 1986 he joined Hewlett-Packard Laboratories in Bristol, England, and in 1989 transferred to his present position.

IEEE Alexander Graham Bell Medal
Arun N. Netravali

Arun N. Netravali (F), director, Computing Systems Research and Technology Conversion Laboratories, AT&T Bell Laboratories, Murray Hill, N.J., is the third recipient of the Alexander Graham Bell Medal.

Netravali joined Bell Laboratories in 1972, became head of the visual communications research department in 1978, and assumed his present position in 1983, with responsibility for high-definition television added in 1990. He holds over 100 patents in such areas as computer networks and digital television.

IEEE Heinrich Hertz Medal
Leopold B. Felsen

Leopold B. Felsen (LF), University Professor, Polytechnic University, Farmingdale, N.Y., has won the Heinrich Hertz Medal "for highly original and significant developments in the theories of propagation, diffraction, and dispersion of electromagnetic waves."

Felsen came to the United States from Germany in 1940 and spent the next three years with a ballistics calibration team in the U.S. Army. He then received the B.E.E., M.E.E., and Ph.D. degrees from the Polytechnic Institute of Brooklyn. Except for a one-year affiliation during 1960–61 as a liaison scientist with the Office of Naval Research in London, Felsen remained with Polytechnic (now the Polytechnic University). He was dean of engineering (1974–78), became Institute Professor (1978–88), and received his present appointment in 1988. His research activities have centered on microwaves, waveguides, antennas, and radar scattering from targets.

Legal aspects

Patent pending: an interactive process

Joel Miller

Intimately involved though engineers are with the creative phase of their work, their exposure to the process of protecting the fruits of their labors is usually brief and limited. Those who apply for patents typically assist with the preparation of the application and rarely participate again. This column will look at the passage of a patent application through the U.S. Patent and Trademark Office and then touch on some aspects of international patent protection.

FIRST STEP. When a patent application arrives at the patent office, it is generally routed to a patent examiner assigned to the pertinent technology. This person will review the application, perform a search for relevant prior patents and publications, and compare the claims against pertinent references, to test for their novelty and unobviousness.

Under the novelty test, a device or process is not new and cannot be patented if exactly the same device or process is disclosed in a prior patent or publication. Under the obviousness test, the claimed invention is also unpatentable if it would have been obvious to one skilled in the technology. Suppose a claim described a solid-state amplifier using a gallium arsenide field-effect transistor (FET). Then if one patent located by the examiner disclosed a vacuum tube amplifier of the same configuration, while another discussed the interchangeability of FETs and vacuum tubes, the examiner could reject the claim as being obvious.

The patents and publications considered by the examiner need not be limited to those found during the examiner's search. Any reference known to the applicant that bears on the examiner's determination of patentability must be provided to the patent office. Otherwise, the resulting patent may be held unenforceable.

If the examiner rejects the claims, the applicant can file a response opposing the rejection or amending the claims or specification to overcome the rejection. But no new matter—material not found in the original application—may be added. Any statements or changes to the claims made by the applicant to secure their allowance should be carefully weighed, as they may limit the scope of the claims. For example, an applicant might represent to the patent office that a proposed claim should be narrowly interpreted to avoid encompassing a cited reference, but then may not later assert a broader interpretation against an accused device even if it satisifies the claim's literal language.

If the claims of an application were previously rejected and the applicant's subsequent arguments do not overcome the rejection, the examiner will likely issue a final rejection. At this point the applicant may submit an "amendment after final," essentially asking the examiner to reconsider, or appeal the rejection, or abandon the application.

SECOND CHANCE. A fourth option after a final rejection is to refile the application as a "continuation" by paying an additional filing fee, maintaining the priority date and obtaining another chance up at bat. A variation of this procedure, a continuation-in-part application (CIP), may be employed where the invention has been modified or improved and the applicant would like to add such features to the application. Here, priority is preserved with respect to material in the original application while the priority date for the new matter is the filing date of the CIP.

If the claims are allowed, the examiner will perform an interference search of related pending patent applications. Should the examiner locate one claiming a similar invention, the patent office will hold an interference proceeding to determine who has priority and is therefore entitled to a patent on the invention.

If the "interference" test is passed, the patent issues for a nonrenewable term of 17 years. In the United States, applicants pay an issue fee followed by periodic maintenance fees to keep the patent in force.

A U.S. patent is effective only within the United States. If an inventor wants protection in another country, Japan, say, or Great Britain, then a patent must be secured in that country as well. It is usual to file first in the country of residence, and then in other countries within the period permitted by international convention, which is generally one year.

Some countries, such as Great Britain, have an absolute novelty requirement, prohibiting any disclosure before filing. If coverage is desired in any of these countries, the applicant must file the initial application before selling a device incorporating the invention, delivering a paper describing the inventions at a professional society meeting, or otherwise publicly disclosing the technical details.

More may be learned about patents from a useful pamphlet titled "General Information Concerning Patents," available for US $2 from the U.S. Government Printing Office, 710 N. Capitol St., Washington, D.C. 20402; 202-275-2091.

Joel Miller is an attorney at the New York City law firm of Weil, Gotshal & Manges.

COORDINATOR: Trudy E. Bell

Engineer at large

Merger in the UK

Two British organizations will unite on Oct. 1 into the United Kingdom's largest engineering institution. The merger between the 110 000-member Institution of Electrical Engineers (IEE) and the 20 000-member Institution of Manufacturing Engineers (IMfgE) is intended to counter the fragmentation of the profession and to strengthen its ability to support innovation and technological development, according to the president of IMfgE, Len Weaver, and the president of IEE, David Jones. The merger is to take effect on October 1 and the new organization will retain the name of IEE.

"The merger is particularly important in the light of the [post] 1992 single European market and will enable us to speak with greater authority to the Government and the EEC [European Economic Community]," said Weaver.

Next comes the creation of a 40 000-member manufacturing division with, it is hoped, a powerful voice in British manufacturing. Later still, another merger is expected in two to three years between the IEE and the Institution of Mechanical Engineers (IMechE).

Prize for a popularizer

Nominations for an award recognizing scientists and engineers who make outstanding contributions to the popularization of science should be submitted by Aug. 1. (They should not be members of the media.) The annual award carries a US $2500 stipend and is sponsored by the American Association for the Advancement of Science (AAAS) and the Westinghouse Foundation. Its goal is to encourage people to popularize their scientific and engineering work and to emphasize the value that the scientific community places on communication with the public. Contributions to be considered include publishing, broadcasting, lecturing, and museum presentation and exhibit design.

The 1991 Award for Public Understanding of Science and Technology will be presented at the AAAS Annual Meeting in Chicago, Feb. 6–11, 1992. *Contact: Patricia S. Curlin, Awards Administrator, Committee on Public Understanding of Science and Technology, American Association for the Advancement of Science, 1333 H St., N.W., Washington, D.C. 20005; 202-326-6602; fax, 202-371-9526.*

COORDINATOR: George Likourezos

Organizations seeking engineers and scientists describe their various openings in the following advertising section

In order to conform to the Age Discrimination in Employment Act and to discourage age discrimination, IEEE may reject any advertisement containing any of these phrases or similar ones, "recent college grads," "1–4 years maximum experience," "up to 5 years experience," or "10 years maximum experience." IEEE reserves the right to append to any advertisement, without specific notice to the advertiser, "Experience ranges are suggested minimum requirements, not maximums." IEEE assumes that, since advertisers have been notified of this policy in advance, they agree that any experience requirements, whether stated as ranges or otherwise, will be construed by the reader as minimum requirements only. While IEEE does not ban the use of the term "entry level," its use is discouraged since, to some, it connotes an age rather than an experience designation. IEEE accepts employment advertising to apprise its members of opportunities. Interested parties should be aware that the political and humanistic values of certain advertisers may differ from their own. IEEE encourages employers to offer salaries that are competitive, but occasionally a salary may be offered that is significantly below currently acceptable levels. In such cases the reader may wish to inquire of the employer whether extenuating circumstances apply.

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Minimum 3 years' design engineering experience in T1, ISDN, data/fax modems, V.32/22/42, DSP, Graphics, Digital Imaging and/or Data Compression. Semiconductor FAE experience is desirable.

Datacom Components

Minimum 3 years' design engineering experience in LANS, Ethernet/802.3, 10BaseT, FDDI and/or fiber optics. Semiconductor FAE experience is desirable.

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Ref No 91266I. The first two years of a Bachelor of Electrical and Electronic Engineering degree course will be offered in 1992 leading to the first engineering graduates from Flinders University in 1994. The course is to be offered within a joint faculty of engineering currently being negotiated with the University of South Australia. Construction of an engineering building has commenced and is expected to be ready for occupancy in late 1991.

A limited term position in electrical/electronic engineering is available from January 1992 for three years with possibility of further two year extension, to teach at undergraduate and postgraduate levels and to develop research activities. Successful appointee will be required to teach from a range of core electrical/electronic engineering subjects concerning basic circuits and systems, measurements, signal processing, computing and control; to develop research activities and to establish links with industry involved in electrical and electronic engineering. Opportunities for consultancy within University guidelines will be encouraged.

Research degree or equivalent professional experience and a strong commitment to the teaching of engineering essential. As teaching in biomedical engineering will begin in 1994, a background and interest in the area of biomedical engineering is desirable.

Further information from the interim Head of the Joint Engineering Programme, Professor Eric Hobson, telephone 61-8-343 3307, fax 61-8-260 4724. Appointment will not normally be made above the sixth level of the scale, viz $A40 257 pa.

Applications, quoting the reference number, and giving full details of qualifications and experience and the names and addresses of three referees of whom confidential enquiries may be made, should be lodged, in duplicate, with [illegible] Manager, Human Resources, The Flinders University of South Australia, GPO Box 2100, Adelaide SA 5001, Australia, by 30 August 1991.

The University reserves the right not to make an appointment or to appoint by invitation.

Equal Employment Opportunity is University Policy

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Calendar

(Continued from p. 12J)

Military Communications Conference–Milcon '91 (COM); Oct. 20–23; McLean Hilton, Virginia; Fay Brady, Mitre Corp., 7525 Colshire Dr., McLean, Va. 22102; 703-883-6733.

Vehicle Navigation and Information Systems Conference–VNIS '91 (VT); Oct. 20–23; Hyatt Regency, Dearborn, Mich.; Mark K. Krage, General Motors Research Labs, Department 18, 30500 Mound Rd., Warren, Mich. 48090; 313-986-2976.

Workshop on Applications of Signal Processing to Audio and Acoustics (SP); Oct. 20–23; Mohonk Mountain House, New Paltz, N.Y.; James Kates, City University of New York, Graduate Center, Room 901, 33 W. 42nd St., New York, N.Y. 10036; 212-642-2179; fax, 212-642-2379.

Advanced Semiconductor Manufacturing Conference and Workshop (ED); Oct. 21–22; World Trade Center, Boston; Margaret Bachmeyer, 2000 L St., N.W., Suite 200, Washington, D.C. 20036; 202-457-9584.

13th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMB); Oct. 31–Nov. 3; Hilton at Walt Disney World, Lake Buena Vista, Fla.; Joachim H. Nagel, Department of Biomedical Engineering, University of Miami, Box 248294, Coral Gables, Fla. 33124; 305-284-2442.

NOVEMBER

International Conference on Computer-Aided Design–ICCAD '91 (ED); Nov. 11–14; Santa Clara Convention Center, Santa Clara, Calif.; ICCAD, 1730 Massachusetts Ave., Washington, D.C. 20036-1903; 202-371-1013.

Third Topical Conference on Emerging Technologies in Materials (ED); Nov. 17–22; Los Angeles Hilton Hotel, Los Angeles; Stevin H. Gehrke, Department of Chemical Engineering, University of Cincinnati, Mail Location 171, Cincinnati, Ohio 45221-0171; 513-556-2766.

DECEMBER

International Electron Devices Meeting (ED); Dec. 8–11; Washington Hilton Hotel, Washington, D.C.; Melissa Widerkehr, c/o Courtesy Associates Inc., 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-639-4990.

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Systems Design Engineer — In this area, you will be involved in guidance and control systems analysis and hardware/software design trade-offs. Specification designs, including guidance, navigation and control algorithm development, as well as systems integration and installation, flight test and customer liaison activity, are a part of these positions.

System Software Development — This area involves development of flight software for advanced guidance and control systems for aircraft using modular and structured programming techniques. You will be involved with algorithms and development of real-time programs in both assembly (8086 family, Z8002 and 68000) and high order languages such as Pascal, "C," Ada and PLM/86, with subsequent hardware integration.

Electronics Engineering — These positions involve the development of new processor/bus architectures and specifications to support fault tolerant/redundant airborne applications.

Display Systems — These positions offer systems, software and hardware opportunities with CRT/LCD display technology. You should be familiar with digital hardware design and/or real-time programming. Systems functions include overall system definition, design and customer interaction.

To qualify for the positions listed above, you should have a BSEE or a BSCS degree and at least three years of experience.

Ada Software Systems Engineers — In these positions you will design, implement and maintain software tools hosted on VAX/VMS computer systems and written in Ada and "C" languages. Experience with designing and implementing compilers, linkers, debuggers and runtime libraries targeted to RISC architectures is required. A background in Ada compiler support is highly desired.

Additional opportunities are available in:

- CRT/LCD Display Technology
- Avionics Systems Simulation
- CAE Engineering (Apollo Mentor Systems)
- Artificial Intelligence
- VAX Systems Administration
- Fiber Optic Pressure Sensors
- EMI/HERF
- Software Tools Development

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Recent books

(Continued from p. 12)

UNIX System V Release 4: The Complete Reference. *Coffin, Stephen,* Osborne McGraw-Hill, Berkeley, Calif., 1990, 905 pp., $29.95.

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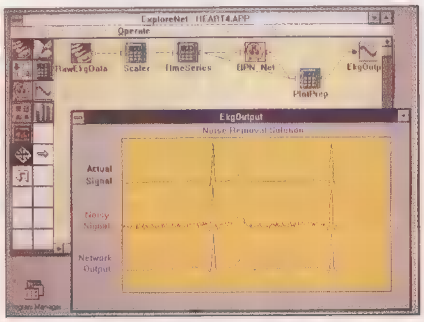
EEs' tools & toys

Neural net software bypasses programming

Two new software packages, ExploreNet 3000 and KnowledgeNet, use neural network techniques to solve engineering and scientific problems without requiring any programming. Instead, the neural network processing scheme is set up through mouse-selectable icons.

Because neural networks exhibit an adaptive behavior that lets them learn from data collected in the past, they do not need algorithms or rules in advance, nor must such things be developed. Instead of being programmed, these networks are "trained" by being exposed to repeated examples of and desired responses to the collected data. Once they are trained, they can "fill in the blanks" for missing data or make predictions.

While the ExploreNet 3000 can solve problems containing large data sets, KnowledgeNet is used in applications calling for yes/no decisions or multiple choices. Both packages require Microsoft's Windows 3.0 running in 386 mode. With Windows'



An ExploreNet 3000 screen shows an application for reducing the noise from a digitized electrocardiogram (EKG) signal. The top trace is the "answer" used during training. The middle trace is the noisy signal. The bottom trace shows the output of the neural network after training.

multitasking capabilities, a user can train a neural network while doing other work in a separate window.

ExploreNet 3000 can be set up to process data according to any of 19 forms of neural networks. The icons needed for this processing include three types of modules: input/output, which specify input files, communicate with other programs, and edit or display textual data; data processing, which contain the neural networks and perform the computations; and display, which allow data to be displayed in text, graph, or image form. Each module may be tailored to application requirements, defined, and tested.

KnowledgeNet's specialty is explaining some of the rationale behind decisions made by a neural network. That information is useful in determining how important any missing data are, what confidence to associate with a decision, and how much each individual input contributes to the decision. KnowledgeNet also comes with a sample program, including a neural network, data, and rationales for making a variety of decisions.

A coprocessor board, the Balboa 860, is also available that can speed applications involving large data sets or pattern recognition by up to two orders of magnitude. These include signal analysis in such areas as medical diagnostics, radar, and sonar, and pattern recognition in industrial process control. According to the manufacturer, HNC Inc., the products get results faster than traditional statistical analysis schemes or programming methods.

Because Balboa 860 brings mainframe computer performance to the execution of the neural network software, it can increase the scope of the modeling and analysis problems the user needs to tackle. Built around the Intel 860 RISC processor, the Balboa 860 board has power equivalent to 40 VAX machines.

Until Aug. 30 the introductory price for ExploreNet is US $750; for KnowledgeNet, $500. Then the prices jump to $1495 and $995, respectively. The Balboa 860 is $10 950. *Contact: HNC Inc., 5501 Oberlin Dr., San Diego, Calif. 92121-1718; 619-546-8877; fax, 619-452-6524; or* **circle 101.**

COMPUTERS

Applying memory cards

An evaluation kit from Databook Inc. can help to develop memory card applications in a wide range of systems and environments. Relying on nonvolatile solid-state memory, the credit-card–sized 3-mm-thick cards are being used to replace rotating magnetic memory in such equipment as notebook computers and other consumer and industrial terminals.

More than 180 computer, software, and semiconductor makers have adopted standards developed for the cards by the PC Memory Card International Association (PCMCIA) in the United States and the Japanese Electronics Industry Development Association (Jeida).

The US $595 kit includes the kit maker's ThinCardDrive memory card drive, a memory card, a connector and mounting hardware, software that runs on a desktop personal computer, and a manual containing both hardware and software design information as well as background information on the joint U.S. and Japanese standard and general "industry trend" information. *Contact: Pete Robson, Databook Inc., Tower Building–Terrace Hill, 112 Prospect St., Ithaca, N.Y. 14850-9952; 716-889-4204; fax, 716-889-2593; or* **circle 102.**

WORKSTATIONS

Glaring guidelines

A guide reprinted by the National Lighting Bureau, *Solving the Puzzle of VDT Viewing Problems*, addresses the problems and solutions of video display terminal (VDT) screen glare. It explains how different forms of glare on the VDT screen prohibit many computer installations from achieving the efficiency, effectiveness, and productivity they could get. It also identifies a range of measures that can be taken to reduce the problem of screen glare, from applying filters and hoods to modifying the workspace environment, reorienting workstations, and adjusting the lighting system.

The guide is available for US $5. *Contact: The National Lighting Bureau, 2101 L St., N.W., Suite 300, Washington, D.C. 20037.*

SOFTWARE

The power of parallelism

A new software package for Turbo C, C//, allows hundreds of independent run-time processes to smoothly cooperate on common resources, self-parallel functions, queues, lists, events, and time-outs. C// contains all the C communications and classical synchronization mechanisms, along with a set of new features, such as a class of semiautomatic variables, run-time control variables, double access to process arguments, stack monitoring, private stacks, and offsets. C//'s dynamic priorities and scheduling facilitate interprocess cooperation.

The package, from Subtlesoft International, can operate over 7000 switches per second on a IBM XT personal computer operating under DOS. It provides a natural platform for pure object-oriented programming, along with such common parallel-oriented problems as real-time control and communication software.

C// costs US $333, and a demonstration kit is available for $33. *Contact: Subtlesoft International, 4344 Bristol St., Pittsburgh, Pa. 15207; 412-521-1158; or* **circle 103.**

COORDINATOR: George Likourezos
CONSULTANT: Paul A.T. Wolfgang, Boeing Helicopters

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EMPLOYMENT OPPORTUNITIES

The following listings of interest to IEEE members have been placed by educational, government, and industrial organizations as well as by individuals seeking positions. To respond, apply in writing to the address given or to the box number listed in care of *Spectrum* Magazine, Classified Employment Opportunities Department, 345 E. 47th St., New York, N.Y. 10017.

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All classified advertising copy must be received by the 25th of month, two months preceding date of issue. No telephone orders accepted. For further information contact Theresa Fitzpatrick, 212-705-7578.

IEEE encourages employers to offer salaries that are competitive, but occasionally a salary may be offered that is significantly below currently acceptable levels. In such cases the reader may wish to inquire of the employer whether extenuating circumstances apply.

Academic Positions Open

Knight Chair in Biomedical Engineering. The Biomedical Engineering Department, University of Miami, invites nominations and applications for its new Knight Chair in Biomedical Engineering. It is expected that candidates will have an outstanding reputation in research, an established record in external funding, and a commitment to education. A person is sought who would establish a strong research link with some branch of the University of Miami School of Medicine. The Department offers M.S. and Ph.D. programs and undergraduate options in other branches of engineering. The University is located in beautiful Coral Gables, within the Miami metropolitan area. Nominations and applications with the names of three references should be sent to Dr. Eugene Eckstein, Biomedical Engineering Dept., PO Box 248294, University of Miami, Coral Gables, FL 33124-0621. The University of Miami is an Equal Opportunity/Affirmative Action employer.

Washington University seeks qualified candidates for the position of Professor and Chair of the Department of Systems Science and Mathematics, with a desired starting date of July 1, 1992. We are interested in outstanding candidates with a strong research record, with a dedication to excellence in undergraduate and graduate education and with ■ demonstrated potential for administration and leadership. Washington University has a long standing commitment to the principle that all candidates should be afforded equal opportunity regardless of age, race, sex or physical disability. Candidates must send a curriculum vitae and a list of references to: Professor C.I. Byrnes, Search Committee for the Systems Science and Mathematics Chair, Campus Box 1040, Washington University, One Brookings Drive, St. Louis, MO 63130.

The Department of Electrical Engineering at Colorado State University is seeking candidates for the Rockwell Optoelectronics Faculty position. This new position will be supported by industry, private endowments, and the University. The position will be a tenured or tenure-track appointment within the Department. We anticipate that the appointment will be for an individual who has recently established an outstanding record of research accomplishments in optoelectronics or a new graduate who shows exceptional promise. Candidates are sought in the areas of optoelectronic semiconductor materials and devices and in optoelectronic systems, with emphasis on practical implementation of telecommunication or optical computing systems. The position will be affiliated with the Center for Optoelectronic Computing Systems (an NSF Engineering Research Center jointly operated with the University of Colorado at Boulder). The new faculty member is expected to develop ■ major research program both through interaction with the existing programs in optical and electronic materials and devices as well as by development of new areas. Applicants should have an earned Ph.D., demonstrated research ability, and a strong interest in undergraduate and graduate teaching. Applicants should submit ■ detailed resume with ■ statement of their professional interests and goals, along with the names of three references. Applications will be accepted until August 31, 1991. This deadline may be extended if suitable candidates are not found. Additional information describing the applicant's work, such as papers or technical reports are welcomed. Please send all application materials to: Professor Jorge I. Aunon, Department of Electrical Engineering, Colorado State University, Fort Collins, CO 80523. (303) 491-6600 Fax (303) 491-2249, Email: aunon@longs.lance.colostate.edu. Colorado State is an EEO/AA employer. Office: 314 Student Services Building.

University of Illinois at Urbana-Champaign. Applications and nominations are invited for the Grainger Professorship in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. The Grainger Professorship has been endowed by The Grainger Foundation, Inc. in honor of Mr. W.W. Grainger who graduated from the College of Engineering in 1919. The appointment will be at the rank of professor with tenure in the Department of Electrical and Computer Engineering. The department solicits applications from distinguished senior engineers with expertise and research interests in any of the following or related areas: power systems, manufacturing, robotics, intelligent systems, control systems, and rotating machinery. Applicants must have an earned Ph.D., outstanding qualifications, and an ability to teach effectively at both the graduate and undergraduate levels. Selected candidates will be expected to initiate and carry out independent research and to perform academic duties associated with our B.S., M.S., and Ph.D. programs. Starting date is negotiable. Salary open, based on qualifications. Send resume, with references and a list of publications to: Professor Chester S. Gardner, Chair, Grainger Professorship Search Committee, University of Illinois, Department of Electrical and Computer Engineering, 1406 W. Green Street, Urbana, IL 61801. (217) 333-2300 The deadline for receipt of application materials to receive full consideration is September 15, 1991. The University of Illinois is an Affirmative Action, Equal Opportunity Employer.

Dean, School of Engineering. University of Alaska Fairbanks. The University of Alaska Fairbanks invites applications for the position of Dean of the School of Engineering. The University of Alaska Fairbanks is the land, sea and space grant campus of the University of Alaska system and the major center of science and engineering research and education. The School of Engineering encompasses three undergraduate academic units (civil, electrical and mechanical engineering) and offers graduate degrees in these disciplines as well as arctic engineering, environmental quality engineering, environmental quality science, engineering management, and science management. The Institute of Northern Engineering, with an annual research budget in excess of two million dollars, is the research arm of the School and is comprised of the Water Research Center, the Transportation Research Center and the Engineering Research Center. Enrollment at the School of Engineering currently includes 350 undergraduate majors and 60 full-time graduate students with 30 full-time faculty. The Dean provides leadership to the faculty and is the chief administrator of the School of Engineering and the Institute of Northern Engineering. The Dean is also responsible for facilitating interactions with other colleges, professional schools and research entities. The UAF campus overlooks Fairbanks, a thriving community of 72,000, rated fourth best small community in the nation. Fairbanks offers outstanding cultural diversity, unsurpassed natural beauty and outdoor recreation, and a friendly local atmosphere. Fairbanks is a transportation hub served by major airlines. Public and private schools in Fairbanks have an excellent reputation. Candidates for this position should have the following qualifications: —Earned doctorate, ■ significant record of both scholarly achievement and sustained research activity sufficient for appointment at the rank of Professor in one of the departments of the School (professional engineering registration is ■ consideration), —Ability to build and maintain strong academic programs and recruit outstanding faculty and students, —Experience in academic and research administration, —Strong communications and human relations skills, —Vision and capability to successfully develop academic and research opportunities in engineering. Send curriculum vitae; statement of interest; and names, addresses, and phone numbers of five references to: Professor Douglas L. Kane, Chair, SOE Dean Search Committee, Water Research Center, School of Engineering, University of Alaska Fairbanks, Fairbanks, AK 99775-1760. Phone (907) 474-7808, FAX (907) 474-6087. Screening of applications will begin 15 July 1991. The anticipated starting date for the position is October/November, 1991. The University of Alaska is an Affirmative Action, Equal Opportunity Employer and educational institution.

The Center for High Technology Materials (CHTM) at the University of New Mexico invites applications for a tenured/tenure track faculty position in Optoelectronics. The specific area of expertise desired is metal organic chemical vapor deposition (MOCVD) of III-V compound semiconductor materials. The successful applicant will work with an existing growth group and other optoelectronics faculty to design growth processes for new optoelectronic devices and would also be expected to establish an independent research program. CHTM presently has one state-of-the-art MOCVD machine and is in the process of acquiring ■ second one. On-going research in the Center includes vertical cavity surface-emitting lasers, laser diode arrays, visible laser diodes, and high efficiency semiconductor laser pumps for solid-state lasers. Rank and salary will be commensurate with qualifications and experience. Send resume and list of three (3) references to: Dr. Brueck, Director of CHTM, University of New Mexico, Albuquerque, NM 87131, before August 1, 1991. The University of New Mexico is an Equal Opportunity/Affirmative Action Employer.

The Department of Systems Design Engineering at the University of Waterloo is seeking applicants for tenure-track positions preferably at the rank of Assistant Professor, to begin employment during 1991-1992 period. The department is interdisciplinary with a diverse range of teaching and research activities which include human systems, societal and environmental systems, systems modelling analysis and design, and intelligent systems. The applicants should have a Ph.D. in Engineering and research interests in one or more of the following fields: 1) Engineering Systems Theory with emphasis in one or more of the following areas: control systems, intelligent systems, modelling and simulation, or system integration and design; 2) Societal and Environmental Systems with emphasis in one or more of the following areas: stochastic and statistical modelling and analysis, optimization, resource allocation, or decision analysis; 3) Environmental System Engineering with emphasis in one or more of the following areas: energy and resource systems

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Membership in the IEEE Engineering Management Society (EMS) is intended to facilitate the transition of engineering professionals to management and contribute to their continued development as managers. Successful managers can keep current on topics in engineering management and related disciplines. Among the many topics EMS has pursued through recent periodic publications and conferences are technology transfer, new product development, organization performance, manufacturing quality and productivity, project risk analysis, and technical growth in Eastern Europe and the Pacific Rrim.

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In today's sophisticated world of information processing, a full range of competitively priced state-of-the-art information-processing systems has been developed to satisfy the spectrum of application requirements. The availability of these systems has led to the predominance of multivendor systems environments—and with it, the urgent demand for multivendor connectivity, system interoperability, and software portability.

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ELECTROTECHNOLOGY IN THE 1992 U.S. R&D BUDGET

This 13-page report prepared for the IEEE-United States Activities' (IEEE-USA's) Technology Policy Council provides an overview of the Bush administration's Federal Fiscal Year (FY 1992) budget request for research and development. In addition to outlining issues that will influence congressional consideration of the budget request, the report highlights proposed funding for electrical and electronics technology programs in the Department of Defense (DOD), the Department of Energy (DOE), the National Aeronautics and Space Administration (NASA), the National Science Foundation (NSF), and the National Institute of Standards and Technology (NIST).

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The IEEE's *1990 Member Opinion Survey* is now available to the public. The survey is an unprecedented worldwide effort by the IEEE to study professional, academic, and intellectual activities of all its members. Previous IEEE surveys were limited to members in the United States.

Among the IEEE-United States Activities programs most important to respondents were professional publications, meetings, workshops, and programs influencing employer practices, the business climate, engineers' public image, and Federal policy. A majority of respondents, both in and outside the United States, urged the IEEE to exert increasingly more influence as a worldwide technical leader.

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modelling and analysis, risk and reliability analysis, environmental impact, or policy development; experience in engineering applications and design is highly desirable. The successful applicants will be expected to teach basic courses in the engineering sciences and mathematics as well as senior level and graduate courses in areas of expertise. Applications with complete curriculum vitae and the names of three references should be sent to Professor M. Chandrashekar, Chairman, Department of Systems Design Engineering, University of Waterloo, Waterloo, Ontario, Canada, N2L 3G1. In accordance with Canadian Immigration requirements, this advertisement is directed to Canadian citizens and permanent residents. The University of Waterloo encourages applications from qualified women and men, members of visible minorities, aboriginal peoples, and persons with disabilities.

New Mexico State University. Tenure and nontenure faculty positions at all professorial and instructor levels are expected to be available with the Department of Electrical and Computer Engineering. A Ph.D. in EE or ECE is required for the professorial ranks and instructor positions are available for qualified doctoral students only. Applications from all areas within EE and ECE will be considered. Send them to Dr. M. Don Merrill, Head, Electrical and Computer Engineering Department, Box 30001, Dept. 3-0, New Mexico State University, Las Cruces, NM 88003. Initial screening will begin July 1, 1991, however, applications will continue to be accepted and evaluated until positions are filled. Positions contingent on eligibility for employment in the U.S. New Mexico State University is an equal opportunity/affirmative action employer.

Post-Doctoral Fellow: The Communication Sciences Laboratory at Simon Fraser University in Greater Vancouver has a post-doctoral opening for research in combined speech and channel coding for digital mobile communications. Candidates should have extensive research experience in at least one of the following areas: speech coding, channel coding and modulation, and mobile communications. The appointment is for one year and can be renewed for another year. The annual salary is in the neighborhood of CDN $25,000. To apply, please send a resume, with names and addresses of three referees, to Dr. Paul Ho, School of Engineering Science, Simon Fraser University, Burnaby, B.C., Canada V5A 1S6.

Dean, College of Engineering, University of Wisconsin-Platteville. The Dean is the chief executive and academic officer of the College and reports to the Vice Chancellor. The College is dedicated to undergraduate education and has 42 faculty, 1400 students and ABET accredited programs in Civil, Electrical, Industrial, and Mechanical Engineering. The ideal candidate must have a PhD in Engineering or a related field. At least one degree must be in Engineering. In addition, the candidate must have demonstrated outstanding administrative and teaching experience with abilities to establish industrial, alumni and community relations. Professional registration and commitment to working effectively with industry, research and fund-raising are desirable. The ability to work with and recruit from a diversified population is essential. The position is available as early as September 1, 1991. For consideration, please submit a letter of application, resume and names, addresses and phone numbers for three references to: Dr. Kenneth Buttry, Chair, Dean Search and Screen, University of Wisconsin-Platteville, Platteville, WI 53818. Women and minorities are especially encouraged to apply. UW-Platteville is an affirmative action, equal opportunity employer.

Faculty Positions—University of Notre Dame. The Department of Computer Science and Engineering at the University of Notre Dame invites applications for tenure track faculty positions at all ranks. Applicants should have a doctorate in Computer Science, Computer Engineering, Electrical Engineering, or a related field. Candidates in all research areas are invited to apply. However, areas of particular interest within the Department are Parallel and Distributed Computing, Parallel Architectures, and VLSI. Applicants should have abilities and interests in teaching at the undergraduate and graduate levels, advising students, and conducting research. Rank and salary are negotiable. Interested persons should forward a complete resume, together with the names, addresses, and telephone numbers of at least three references, to: Dr. Steven C. Bass, Chairman, Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, IN 46556. The University of Notre Dame is an Affirmative Action/Equal Opportunity Employer.

Graduate Research Assistantships are available in electrical engineering at the University of New Mexico Center for High Technology Materials. Research activities include development and application of metal-organic chemical vapor deposition for infra red and visible diode laser materials. Entry level M.S. and Ph.D. candidates will be considered. Must have strong technical background with industrial experience preferred. Send resume to Prof. C.F. Schaus, Rm L216B, University of New Mexico, Albuquerque, NM 87131.

The Electrical Engineering-Electrophysics Department of the University of Southern California invites applications for tenure-track faculty positions in Antennas and Applied Electromagnetics, Quantum Electronics, Photonics, Lasers and Optics, Optoelectronics, VLSI Circuits and Systems, and Power System Devices. Candidates must have Ph.D. and strong interest in teaching, research, and supervising M.S. and Ph.D. candidates. Resume and names of three references should be sent to Prof. H.H. Kuehl, Chair, EE-EP, PHE 604, University of Southern California, Los Angeles, CA 90089-0271.

The Center for Telecommunications Research (CTR) at Columbia University has an opening for an associate research scientist position. Ph.D. in Electrical Engineering or Computer Science is required. The successful candidate is expected to focus on object-oriented distributed database and operating system aspects of the traffic control architecture of giant integrated networks. Strong track record in software for ultrahigh-speed networks and real-time systems is a plus. Knowledge of Transputers is desirable. Send resumes to: Aurel A. Lazar, Center for Telecommunications Research, Columbia University, New York, NY 10027. Columbia University is an Equal Opportunity Employer.

Graduate Research Assistants. The Center for Microelectronics Research (CMR) at the University of South Florida is seeking graduate research assistants to support research activities in the areas of microelectronic materials and defects, semiconductor processing, and VLSI/ULSI architecture, circuit design and test. Successful applicants will be required to pursue a PhD Program in E.E., Computer Science, or Physics. Stipends are available in the range of $12K to $16K (half time) for a full calendar year with tuition waivers available. Applicants must have an excellent academic record and a minimum of a Bachelors degree in an appropriate discipline. CMR research funding totals nearly $10M over the past two years with primary support coming from state, DOD and industrial funding sources. USF is an Affirmative action/equal opportunity employer. Requests for information or resumes should be directed to Dr. Earl Claire, Acting Director, CMR/USF College of Engineering, 4202 Fowler Ave., Tampa, FL 33620. (813) 974-2096.

Biomolecular Engineering, College of Engineering and Technology, Ohio University. Applications are invited for a tenure track faculty position in Biomolecular Engineering at the rank of Assistant Professor. Applicants should have a Ph.D. with an outstanding academic record in an engineering or related discipline. The successful candidate will participate with an active group in extending the Biomolecular Engineering area within the College of Engineering and Technology and develop a research program of national recognition on the synthesis of recombinant proteins and peptides, their large scale production and separation. A strong commitment to both undergraduate and graduate education is expected. Ohio University has an established, internationally renown program in Molecular and Cellular Biology which, together with the Edison Animal Biotechnology Center, provides a unique opportunity for the foundation of a highly successful Biomolecular Engineering Program. A special new building to house the program is already in the planning stage and the new faculty will have the opportunity to work closely with architects to provide a state-of-the-art engineering facility. Substantial start-up funds are available. A resume, a brief summary of research experience and plans and names of at least three references, should be sent to Prof. W.P. Jepson, Chairman of Chemical Engineering Department, Stocker Center, Ohio University, Athens, Ohio 45701. Applications will be accepted until September 15 1991, or until position is filled. Ohio University is an Equal Opportunity and Affirmative Action Employer.

The University of Saskatchewan invites applications for a tenure track position in the Department of Electrical Engineering. Appointments are normally made at the Assistant Professor level. The candidate will join the Communications Research Group and will work with NSERC Chair in Communications. Preference will be given to candidates in the field of digital communication with specialization in RF, Microwave or Optical circuits/systems. Alternatively, candidates in coding, modulation or equalization theory for communication channels will be considered. Applicants must hold an earned Ph.D. degree and have demonstrated potential for teaching at the undergraduate and graduate levels and for developing an independent research program. The Department offers programs leading to B.E., M.Eng., M.Sc., and Ph.D. degrees. There are approximately 150 undergraduate and 60 graduate students in the Department and excellent research facilities. Curriculum vitae, a list of three referees and a statement of research interest should be addressed to: Dr. M.S. Sachdev, Head, Department of Electrical Engineering, University of Saskatchewan, Saskatoon, Canada, S7N 0W0. Applications must be received by September 30, 1991. The expected appointment date is January 1, 1992. In accordance with Canada Immigration regulations, this advertisement is directed in the first instance to Canadians, but other qualified candidates are also encouraged to apply.

George Mason University. The Center of Excellence in Command, Control, Communications, and Intelligence (C3I) was established by Dr. Harry L. Van Trees at George Mason University two years ago. The Center is an interdisciplinary research center within the School of Information Technology and Engineering that is committed to the establishment of an intellectual basis for the investigation and application of C3I principles in the context of federal, military, industrial, and commercial environments. The Center conducts a broad spectrum R&D program including projects in sensing and data fusion, image compression, neural networks, command support systems, automated planning, communications networks, signal processing, adaptive arrays, multilevel security, C3 architectures, Petri nets modeling and simulation, photonics, software engineering, and corporate information management systems. Currently 22 faculty and 50 graduate students are associated with the Center, and research awards will exceed 5 million dollars this year. The majority of the Center faculty has academic appointments in one of the five departments in SITE and research appointments in the C3I Center. Three types of appointments are currently available. Tenure track and tenured appointments are available in the Systems Engineering Department. Applicants must have a Ph.D. plus a minimum of 5 years experience in one of the following areas: sensor and data fusion, structured analysis techniques, or modeling and simulation. Tenure track appointments are available in the Electrical and Computer Engineering Department. Applicants must have a Ph.D. with emphasis in computer systems architecture, VLSI, or communications. Postdoctoral and research faculty appointments are available in any of the areas listed above. Applicants should send a complete resume in-

dicating the position for which they are applying and include the name and address of three references to Dr. Harry L. Van Trees, Director, C3I Center, George Mason University, 4400 University Drive, Fairfax, Virginia 22030. George Mason University is an equal opportunity/affirmative action employer, and actively seeks the candidacy of women and minorities.

Government/Industry Positions Open

Electrical and Computer Engineers—Fish & Neave is a nationally known intellectual property law firm of over 100 lawyers located in midtown Manhattan. We are seeking graduate students or practicing engineers, preferably with advanced degrees, in the areas of electrical engineering and computer technology who are interested in the field of patent law for our Patent Agent Trainee program. We offer full-time employment, in which we train the individual to prepare and prosecute patent applications and perform other tasks relating to our practice, including litigation, while attending night law school in the New York City area. Salary: Not less than $55,000/yr. Benefits: Full law school tuition; full medical benefits; four weeks paid vacation. Send resumes to Deirdre M. Rogan, Recruitment Coordinator, Fish & Neave, 875 Third Avenue, New York, NY 10022-6250.

Senior Systems Engineer needed to direct, coordinate, design, and develop computer hardware and software in the areas of signal processing, high speed data acquisitions and process control. Plan and formulate engineering programs and organize project staff according to project requirements utilizing Digital Equipment and DEC hardware, and computer languages including C, UNIX/XENIX, and UNIFY/ACCELL, RDRMS. Assign project personnel to specific phases or aspects of project, such as technical studies, product design, preparation of specifications and technical plans, and product testing. Evaluate and approve design changes specifications, and design releases. Review product design for compliance with software and hardware engineering principles, company standards, and customer contract specifications. Requires a Bachelor's degree in Electrical Engineering and two years experience in job offered or two years directly related experience using the UNIFY/ACCELL and UNIX/XENIX Systems. 40 hour work week. $40,000 per year. Apply at the Texas Employment Commission, Dallas, Texas, or send resumes to the Texas Employment Commission, TEC Building, Austin, Texas 78778. Job Order #6342744. Ad paid by an Equal Employment Opportunity Employer.

Transformer Design Engineer—Design of 10-1300 MVA power transformers. Compose instructions to drafting department for preparation of manufacturing and user drawings. Draft instructions to manufacturing facilities for design testing and processing. B.S. required in Electrical Engineering. Must know transient analysis of capacitive-inductive circuits; thermal calculations; determination of magnetic shielding; short circuit modeling; field plotting techniques; and insulation of high voltage dielectric structures in power transformers. 40 hrs./wk. [illegible] a.m.—5 p.m. $38,400/yr. Send resume with Social Security number to Indiana State Employment & Training Services, 10 North Senate Avenue, Indianapolis, IN 46204 Attention W.F. Shepherd. Refer to I.D. 3288157.

Automation Systems Engineer—For Roanoke, VA. area Emp. Resp. for auto. eng. for metals ind. process control sys. Duties inc. comp. sys. requirement analysis, software functional def. and design specs., software eng. for real time ind. control funcs., sys. integration and func. testing, & factory support of auto. installations in metals ind. Must have M.S. or equiv. in Elec. Eng. w/6yrs. wrk. exp. in metals ind. auto. eng. Must have exp. w/VAX/VMS comp. sys. hdw./sftw. & prof. in Fortran and ADA prog. lang., sftw, eng. methodology and metals processes and operation. 40 hrs./wk. Hrs. 8:00-4:45, $37,200/yr. No OT. To apply: mail or hand carry Res. w/copy of Ad. to: VEC, Dept. 3008, 1202 Franklin Rd., Roanoke, VA 24002-0061, J.O. [illegible] VA0021283. EEOE.

Automotive Product Engineer with an Engineering Consulting firm. Duties include design, development, and testing of electronic engine control systems for gasoline fueled vehicles; -develop and analyze technical data by testing of vehicle components and systems; -design and develop test procedures and programs, organize and schedule testing; -formulate engineering conclusions and make recommendations; -evaluate proposed engine control systems; -write technical reports; -extensive use of personal computer for above functions. Requires a Bachelor's Degree in Electrical Engineering to include at least one course, or project in electronic engine control systems. Also requires five years experience in the job offered or five years experience as an electrical engineer, work experience to include development of electronic control systems. Hours are from 7:00 a.m. to 3:45 p.m., forty per week. Salary is $38,000 per year. Send resume to 7310 Woodward, Room 415, Detroit, MI 48202. Refer to #33491.

Engineering—Senior Manufacturing Systems Engineer. Responsibilities include the following four projects: 1) Automated Material Handling Expansion—support development of system configuration (AGVS systems, Stocker systems, and robotics) through use of simulation design engineering tools, validate designs through computer simulation and other analytic tools, and help ensure system meets user requirements; 2) PRI Intrabay Robotics—help prove the technical viability of using PRI robotic system for future intrabay automated material handling projects through system performance verification, software integration, and acceptance testing of the monorail system, the stocker systems and robotics; 3) Automated Material Handling—support development of system configuration (Monorail systems, AS/RS systems, and SWRs) through simulation design engineering tools, validate design through computer simulation and other analytic tools, and provide expected performance indicators; and 4) Interbay Intrabay Automated Material Handling - support project team in defining appropriate robotic transportation systems and storage systems for sub-micron fab, perform value engineering and systems engineering functions on potential design options through simulation technology. Requires Ph.D. in Industrial Engineering. Requires background in simulation engineering with emphasis in manufacturing. Knowledge of C and/or Lisp, and one major simulation language required. Knowledge of UNIX operating system essential. Requires academic or practical background in design of experiments, simulation model development, verification, and validation of model results, as well as object-oriented programming skills in simulation with special emphasis in manufacturing-based simulators. Must be able to market technical ideas effectively. $4,475.00/month; 40 hours/week. Place of employment and interview: Chandler, Arizona. If offered employment, must show legal right to work. Clip ad and send with resume to Job. No. S719. P.O. Box 58-119, Mailstop GR1-57, Santa Clara, California 95052-58119, not later than July 11, 1991. The Company is an equal opportunity employer and fully supports affirmative action practices.

Executive Officer: 60% to full-time position (start 1/1/92) in nonprofit technical society. Attendance (expenses pd) at 10/30/91 meeting in Orlando required. Candidate must have experience as manager of nonprofit technical society, as volunteer in same, or as administrator in technical area. Advanced degree and knowledge of IEEE procedures and Biomedical Engineering desirable. Flexible working hours and location. Major equipment provided. Contract position. Send enquiries to IEEE/EMBS, P.O. Box 2477, Durham, NC 27715 by 8/15/91.

Sr. Technology Engineer. Resp. for developing new process flows for each new generation of BICMOS technology & defining reqs. for new process steps needed. Work involves application of semiconductor materials & device characterization techniques for identification of device parameters & technology limitations; design & execution of experiments for process & device optimization; support of process transfer to production; identification of technology related factors limiting production yield; & recommendation of solutions to production difficulties associated with technology. Reqs. Ph.D. in Elec. Engrg. & 1 yr. exp. in job offered or in research & development related to semiconductor materials & devices. Also reqs. knowl. of semiconductor characterization techniques in general, & specifically with dopant profiling methods, electron microscopy, & electrical characterization of devices; exp. with semiconductor processing, in particular as applied to fabrication of BIPOLAR devices; & know. of process, device, & circuit simulation, & device parameter extraction. Salary: $53,000/yr. Job & interview site: San Jose, CA. Send ad with resume to PO Box 641392, San Jose, CA 95164-1392 not later than July 31, 1991.

Project manager for NE Ohio engineering firm to design and develop electrical distribution systems and communications systems for international commercial, industrial and residential engineering projects utilizing both the U.S. National Electrical Code and the British Standard Specifications. Consult with local authorities with regard to code requirements and regulations. Purchase all electrical materials and components used in projects. Prepare maintenance manuals and instruct clients' maintenance engineers in system functions and maintenance. Supervise integration and completion of projects. 4 yrs. experience in electrical engineering; MS degree in Electrical Engineering. Degree must have included one graduate level course each in Power Systems, Theory of Electric Machines, and Control Engineering. Must be able to travel to middle East and Africa, travel not to exceed 40% of time. Must be able to speak, read, and write Arabic. Experience must have included 1 yr. working with British Standard Specifications. Mon-Fri, 8am-4:30pm, $40,190/yr. Must have proof of legal authority to work permanently in U.S. Send resume in duplicate (No Calls) to S. Holton, JO# 1239970, Ohio Bureau of Employment Services, P.O. Box 1618, Columbus, Ohio 43216.

Electronics Design Engineer—A leading Chicago area manufacturer of high quality, precision electronics components for the medical electronics marketplace is seeking a senior electronics design engineer. This position will involve the design of analog and microprocessor based equipment from specifications. Exposure to audio design would be helpful. In addition to project level design responsibilities, this key individual will provide technical manufacturing support to existing products. As you might expect, we need a BSEE degreed individual with about 5-10 years of solid, microelectronics, product development experience. Since this is a senior level position we need someone with excellent analytical abilities along with practical troubleshooting skills. This position offers an opportunity to work within a sophisticated and advanced technical environment along with a competitive compensation and benefit package. Please send a resume in confidence to: IEEE Spectrum, Box 91-02, 345 East 47th Street, New York, NY 10017. Equal Opportunity Employer m/f.

Project Engineer for rate responsive cardiac rhythm control devices to direct 3-4 design, mech. & tech. engineers on the design & development of advanced implantable rate responsive pacemakers/defibrillators & auxiliary equipment: assigns each to specific phase or aspect of project. Responsible for planning, organization, control, integration & completion of project; oversees development of tech. product specs while negotiating with marketing staff. Serves as R&D liaison to clinical, regulatory affairs, marketing & manufacturing to provide tech. engineering support, interpretation of test results & ensure compliance with FDA. Evaluates & approves design changes, specs & drawing releases; coordinates activities re: tech. developments, scheduling, & resolving engineering design & test problems; prep. of interim & completion project reports; controls expenditures within limit of project budget. Requires: B.S. degree in Electrical Engineering; 2-3 yrs. exp. in above duties or 3-5 yrs. as Electrical Design Engineer for implantable cardiac life support systems with emphasis on design of integrated circuits; working knowledge of cardiac pacemaker & defibrillator technology, rate-responsive technology & principles, high reliability requirements for implant-

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EMPLOYMENT OPPORTUNITIES

able cardiac life support systems, cardiac electrophysiology & pathology & physiology, telemetry systems for programming pacemakers, automated design tools, & software programming in "C" & "assembly" language. Salary: $51,000 per yr. 40+ hrs. per wk. Application by resume. Send resume to: Colorado Dept. of Labor & Employment, 600 Grant Street, Suite 900, Denver, CO 80203-3528. Referring to J.O. CO3195441.

Systems Consultant Engineer for industrial software service and system integration company in NE Ohio. Design computer integrated manufacturing system, e.g. process control, automatic control manufacturing facilities and management information systems for industrial clients; analyze client's requirements to define control objectives, establish control system models, develop control strategies and implement control systems using programmable logic controllers, process computers and distributed control systems, which includes specification of hardware components and software packages, design applications software and development of communications network for the control system, testing documentation and supervise installation. Must have M.S. in systems engineering or electrical engineering. Applicant must have 1 year experience in the job described. In lieu of 1 year experience in the job described, applicant may have 1 year training or work experience or any combination thereof using programmable controllers. This training or work experience may be gained before during or after degree. Applicant must also have at least one graduate level course in each of the following: fundamentals and techniques of static and dynamic optimization, industrial process control and one undergraduate course in drive control systems, microprocess computer control technology. 40 hrs/wk 8-12am 1-5pm Mon-Fri, $35,500 per annum. Must have proof of legal authority to work permanently in U.S. Send resume in duplicate (no calls) to S. Holton, JO#1255718 Ohio Bureau of Employment Services, PO Box 1618, Columbus OH 43216.

Government/Industry Position Wanted

Innovative & versatile Ph.D. (Power & System analysis), 30 years experience in Utility R&D (Systems, reliability, economics, HV, & high current), Govt. agency, Regulation, and steel industry, several publications: seeks Utility/Consulting Engineering/Industry/R&D, or academic position. Responses to: IEEE SPECTRUM, Box 91-01, 345 East 47th Street, New York, NY 10017.

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In July 1991, the Nanyang Technological Institute (NTI) will be reconstituted and renamed the Nanyang Technological University (NTU). It will conduct a wide range of courses at degree and postgraduate levels.

The School of Applied Science currently offers undergraduate degree courses in COMPUTER TECHNOLOGY and MATERIALS ENGINEERING. Applications are invited from suitably qualified persons to fill teaching positions in the following areas:

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1. Microprocessor-Based System Design
2. Computer Architectures
3. Advanced Microprocessors
4. Computer Communications
5. CAD/Computer Graphics
6. Real-Time Systems
7. Computer Peripherals
8. Control & Instrumentation
10. Image Processing/Computer Vision
11. Artificial Intelligence
12. VLSI System Design
13. Robotics
14. Compiler Design
15. Distributed Computing
16. Fault-Tolerant Computing
17. Performance Prediction & Analysis

Preference will be given to applicants with expertise in both hardware and software

MATERIALS ENGINEERING

1. Metal Casting
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3. Welding
4. Electronic and Magnetic Materials
5. Surface Treatment
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7. Failure of Materials
8. Materials Selection and Design Considerations
9. Modern Analytical Examination of Materials
10. Metal Working and Forming
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14. Ceramics
15. NDT Techniques
16. All aspects of Physical Metallurgy

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Applicants should possess a good Honours degree and a relevant higher degree. Preference will be given to those with teaching/research or industrial experience. Appointees will be expected to initiate and take part in research programmes and to participate in academic/professional activities that complement the industrial development of Singapore.

Gross annual emoluments range as follows:

Lecturer	: S$ 53,160 - S$ 64,200
Senior Lecturer	: S$ 58,680 - S$100,310
Associate Professor	: S$ 88,650 - S$122,870
Professor	: S$108,870 - S$146,970

(US$1.00 = S$1.73 approximately)

In addition to the above, the Institute adopts the Government's practice in the payment of a variable bonus, the quantum of which is tied to national economic performance and has, in past years, ranged from 1 to 2 7/8 months of December salary.

The commencing salary will depend on the candidates' qualifications, experience, and the level of appointment offered.

Leave and medical benefits will be provided. Depending on the type of contract offered, other benefits include: provident fund benefits or an end-of-contract gratuity of 25% of the staff member's last drawn monthly salary for each completed month of service, a settling-in allowance, subsidised housing, education allowance up to a maximum of S$30,000 per annum, passage assistance, baggage allowance and car loan.

The Institute encourages its staff to undertake outside consulting work of a specialist nature. They are permitted to earn and retain such consultation fees up to a maximum of 60% of their gross annual emoluments in any one calendar year.

Campus

The Institute has a modern campus with up-to-date facilities for teaching and research as well as residential and recreational facilities for staff and students. It has one of the largest high-speed campus wide network of computing facilities for supporting teaching, research and office automation in this region. Over a hundred engineering workstations and a thousand PCs are supported on NTInet which runs into all academic staff offices and laboratories. Large computation and file servers available on NTInet include three large VAX8820s, one VAX8530, one VAX8200, five VAX3500 servers and ten MicroVAX II servers. In addition dedicated CAD/CAM facilities are available in the various Schools. The Institute also provides its users with a communication link via NTInet to a supercomputer installed in the Singapore Science Park.

Further information on the above may be communicated to the Institute through **BITNET to:TFWANG@NTIVAX**

Candidates wishing to be considered should write to:

THE DIRECTOR
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Scanning
The Institute

Is MRI safe?

Some medical researchers are now saying that, with the advent of faster and more powerful systems, magnetic resonance imaging (MRI) safety should be given more attention. Their discussions at a recent conference on the safety issue focused on biological effects as well as accidents [THE INSTITUTE, July/August, p. 1].

A push for gallium arsenide ICs

As designers of communications products eye frequencies above 2 GHz, they are spurring interest in gallium arsenide ICs, which, unlike silicon ICs, can operate at those frequencies [THE INSTITUTE, July/August, p. 1].

Presidential candidates speak out

A second installment of THE INSTITUTE's poll of the IEEE President-Elect candidates in this fall's annual election presents the four candidates' views on representation, industry support, electrotechnical leadership, and member services [THE INSTITUTE, July/August, p. 8].

NSF funds five engineering centers

The National Science Foundation (NSF) has granted five-year, renewable awards of up to US $16.8 million each to five Engineering Research Centers at Columbia University, the Massachusetts Institute of Technology, Purdue University, the University of Maryland, and Duke University [THE INSTITUTE, July/August, p. 2].

Laser pumps colors from silicon

Researchers at Britain's Defense Research Agency in Malvern have produced silicon-based semiconductors capable of emitting red, orange, yellow, or green light after being illuminated by higher-frequency laser radiation in the green, blue, or ultraviolet region [THE INSTITUTE, July/August, p. 6].

Canada buys most U.S. electronics

Canada is the United States' best customer for electronics, buying more than $12.5 billion worth of products in 1990, according to the Electronic Industries Association, Washington, D.C. Japan is second ($8.4 billion) and the United Kingdom is third ($6.2 billion). Japan is the top supplier of electronic products to the United States ($30.6 billion), followed by Singapore ($6.9 billion) and Taiwan ($6.3 billion) [THE INSTITUTE, July/August, p. 3].

Zinc-air battery powers best car

Four zinc-air battery stacks containing 33 cells each powered the winning electric vehicle at the First Annual Solar and Electric 500 auto race, held in Phoenix, Ariz. [THE INSTITUTE, July/August, p. 6].

Nuclear and gas power favored

Over the next 20–30 years nuclear and natural-gas-fired plants are likely to win favor as the most economical and safe ways to generate electricity. That was the conclusion of interdisciplinary experts who met in Helsinki in May to assess how best to appease the world's growing hunger for electricity [THE INSTITUTE, July/August, p. 1].

Coming
in Spectrum

What's next for NASA? The debacles and errors of the space program in recent years have many people wondering what is wrong with NASA's organization. Meanwhile, Europeans have commandeered up to half the world's commercial space launch business. And now President Bush is ordering a multiagency effort for space exploration, involving the departments of Defense and Energy as well as NASA. This special report examines three questions:

- How does the U.S. space program compare with those of other countries?
- Does Bush's multiagency mandate change things or merely ratify the status quo?
- Do NASA's present difficulties differ from those of the Apollo era?

What's new in LANs? The extensive nature of electrical engineering activities is persuading many companies to invest in local-area networks (LANs) so that their engineers, however far apart geographically, can share design data, confer, and remotely control manufacturing. This focus report covers such developments in data communications as:

- High-speed LANs: FDDI, 802.6, and more.
- LAN interconnection: using bridges, routers, and gateways. Evolving Frame Relay and SMDS (switched megabit data services) are also addressed.
- High-speed networks like the broadband integrated-services network (BISDN) and the synchronous optical network (Sonet).

Also included are tables of representative high-speed LAN and LAN interconnection systems, as well as tables of prototype BISDN switches and integrated circuits for Sonets.

Look, no magnet. In 1820, when Oersted deflected a magnetic needle by moving a current-carrying wire next to it, he began the era of magnetism without magnets. This article is part of the Back to Basics series.

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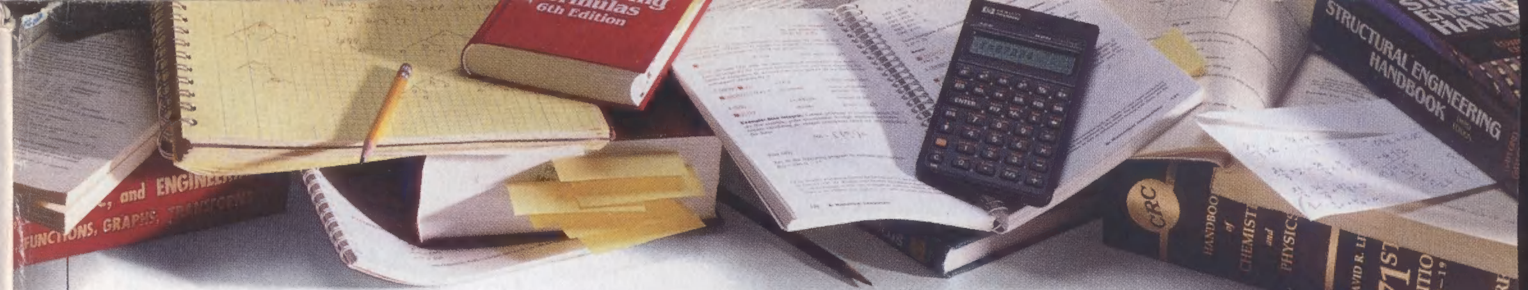

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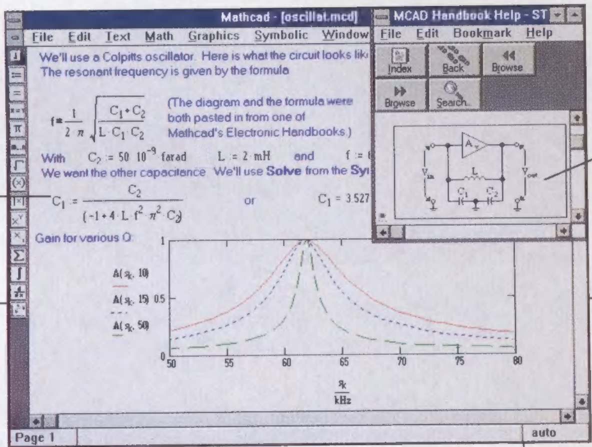

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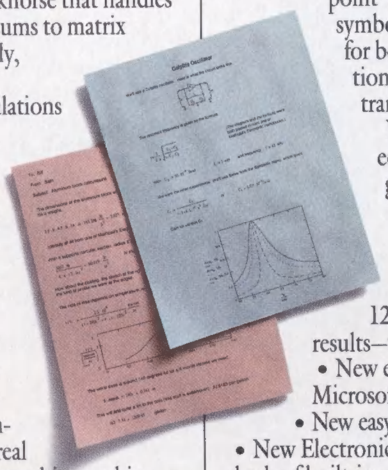

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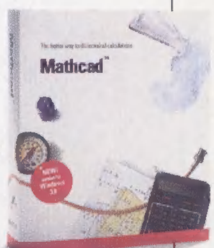

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